


SYNC MASTER=T18 MLB

SYNC DATE=12/12/2007

System Block Diagram

 Apple Inc.

051-7898

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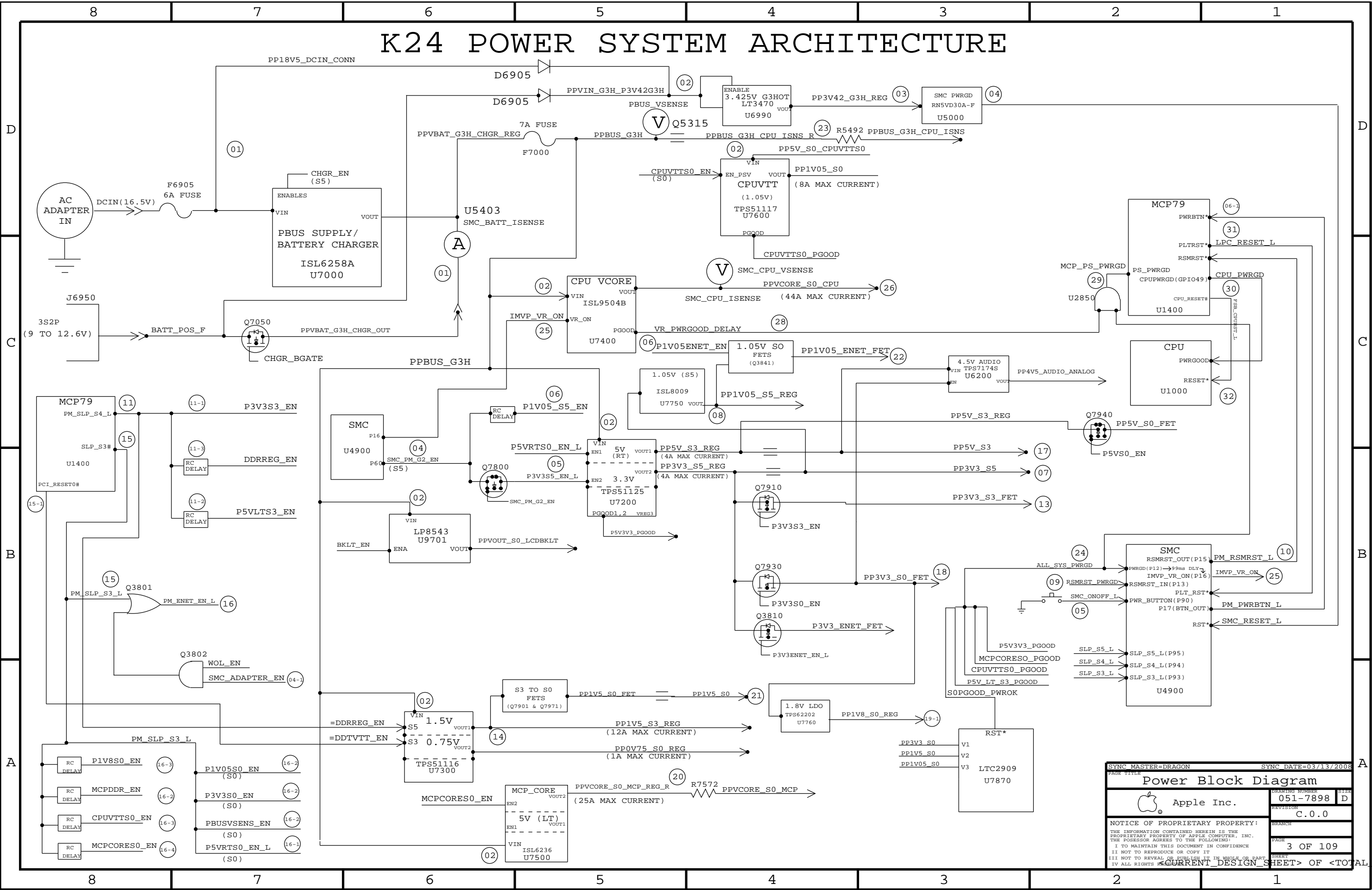
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9923	PCBA,MLB,BETTER,K24	K24_COMMON,CPU_2_26GHZ,EEE_6GC,KB_BL
630-9924	PCBA,MLB,BEST,K24	K24_COMMON,CPU_2_53GHZ,EEE_6GD,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6G4]	CRITICAL	EEE_6G4
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6GC]	CRITICAL	EEE_6GC
826-4393	1	LRL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:6GD]	CRITICAL	EEE_6GD

BOM Groups

BOM_GROUP	BOM_OPTIONS
K24_COMMON	COMMON,ALTERNATE,K24_MCP,K24_MISC,K24_DEBUG_PROD,K24_PROGPARTS
K24_MCP	MCP_B03,BOOT_MODE_USER,MCPSEQ_SMC
K24_MISC	ONEWIRE_PU,DP_ESD,MIKEY,BKLT_PROD,SUPERCAP_NO,LDO_NO
K24_PROGPARTS	BOOTROM_PROD,SMC_PROD,IR_PROD,WELLSPRING_PROD
K24_DEBUG_ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K24_DEBUG_PVT	DEVEL_BOM,BMON_PROD,SMC_DEBUG_YES,XDP,NO_VREFMRGN
K24_DEBUG_PROD	BMON_PROD,SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN
K24_DEVEL_ENG	BMON_ENG,XDP_CONN,LPCPLUS,VREFMRGN,FWPHY_WAKE_YES
K24_DEVEL_PVT	LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM_OPTION
337S3646	1	PDC, SLOBE, PRQ, 2.0, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3704	1	PDC, SLOE2, PRQ, 2.26, 25W, 1066, RO, 3M, BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC, SLO4H, PRQ, 2.4, 25W, 1066, MO, 3M, BGA	U1000	CRITICAL	CPU_3_4GHZ
337S3756	1	PDC, SLOF0, PRQ, 2.53, 25W, 1066, RO, 3M, BGA	U1000	CRITICAL	CPU_2_53GHZ
337S3761	1	PDC, SLOG0, PRQ, 2.66, 25W, 1066, RO, 3M, BGA	U1000	CRITICAL	CPU_2_66GHZ
338S0710		IC, OMCP, MCP79, 35X35MM, BGA1437, B03	U1400	CRITICAL	MCP_B03

Programmable Parts

338S0563	1	IC, SMC, HSB/2117, 969MM, TLP, HF	U4900	CRITICAL	SMC_BLANK
341S2445		IC, SMC, K24	U4900	CRITICAL	SMC_PROG
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2441		IC, PROGRAM, EFI, BOOTROM, UNLOCK, K24	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC, CY7C63839, ENCORE II, USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093		IC, IR CONTROLLER, M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC, P80C+ W/ USB, 56 PIN, MLF, CYRCC24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2503	1	IC, PROGRAM, WELLSPRING CONTROLLER	U5701	CRITICAL	WELLSPRING_PROG

LOCKED BOOTROM APN IS 341S2443

Alternate Parts


PART NUMBER	ALTERNATE PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISRAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MACLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MACLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7555 CPU AS ALTERNATE
353S2718	353S2310		ALL	INTERTEC AS ALTERNATE

DEVELOPMENT BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0741	1	K24 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K24 BOARD STACK-UP

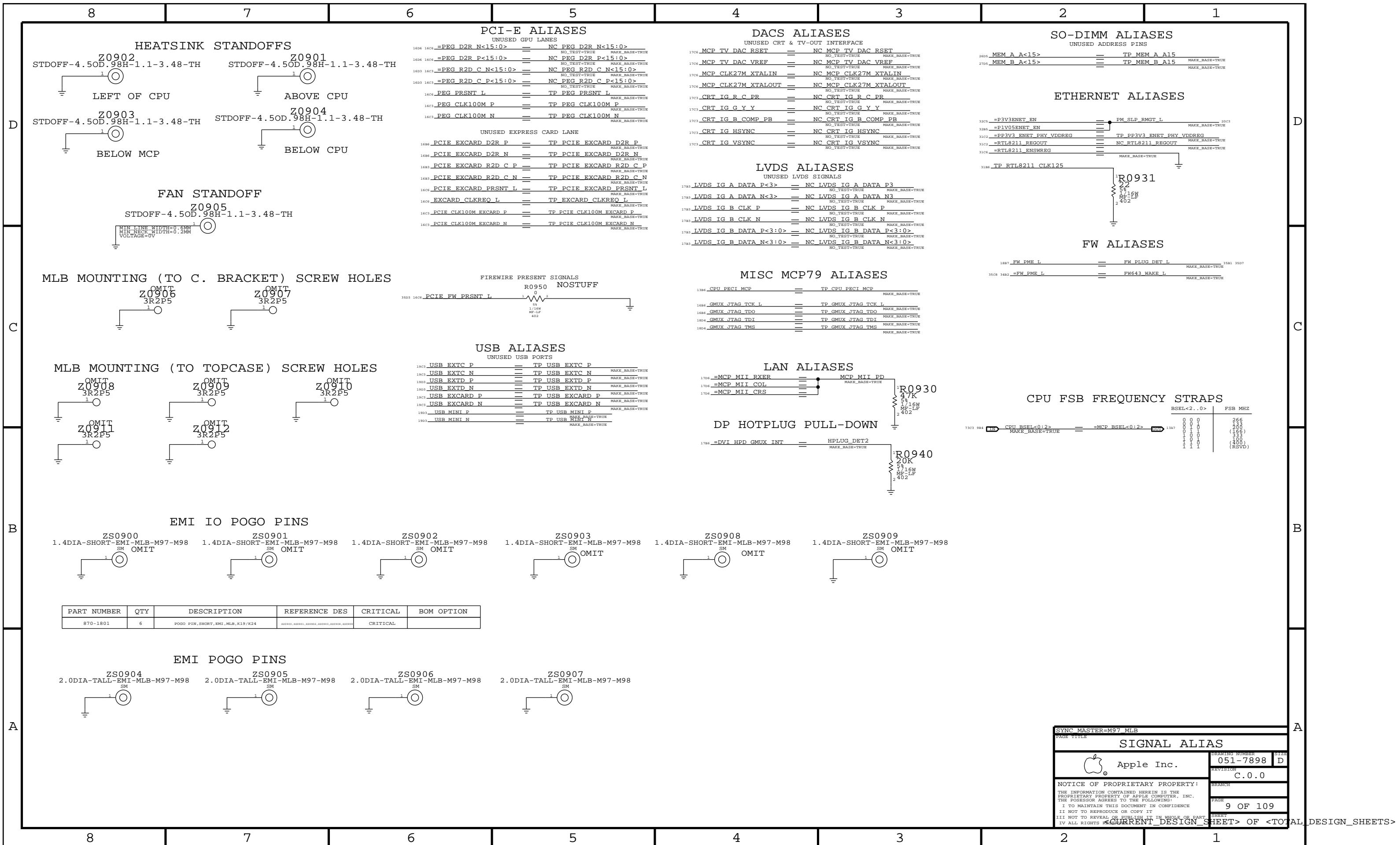
Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

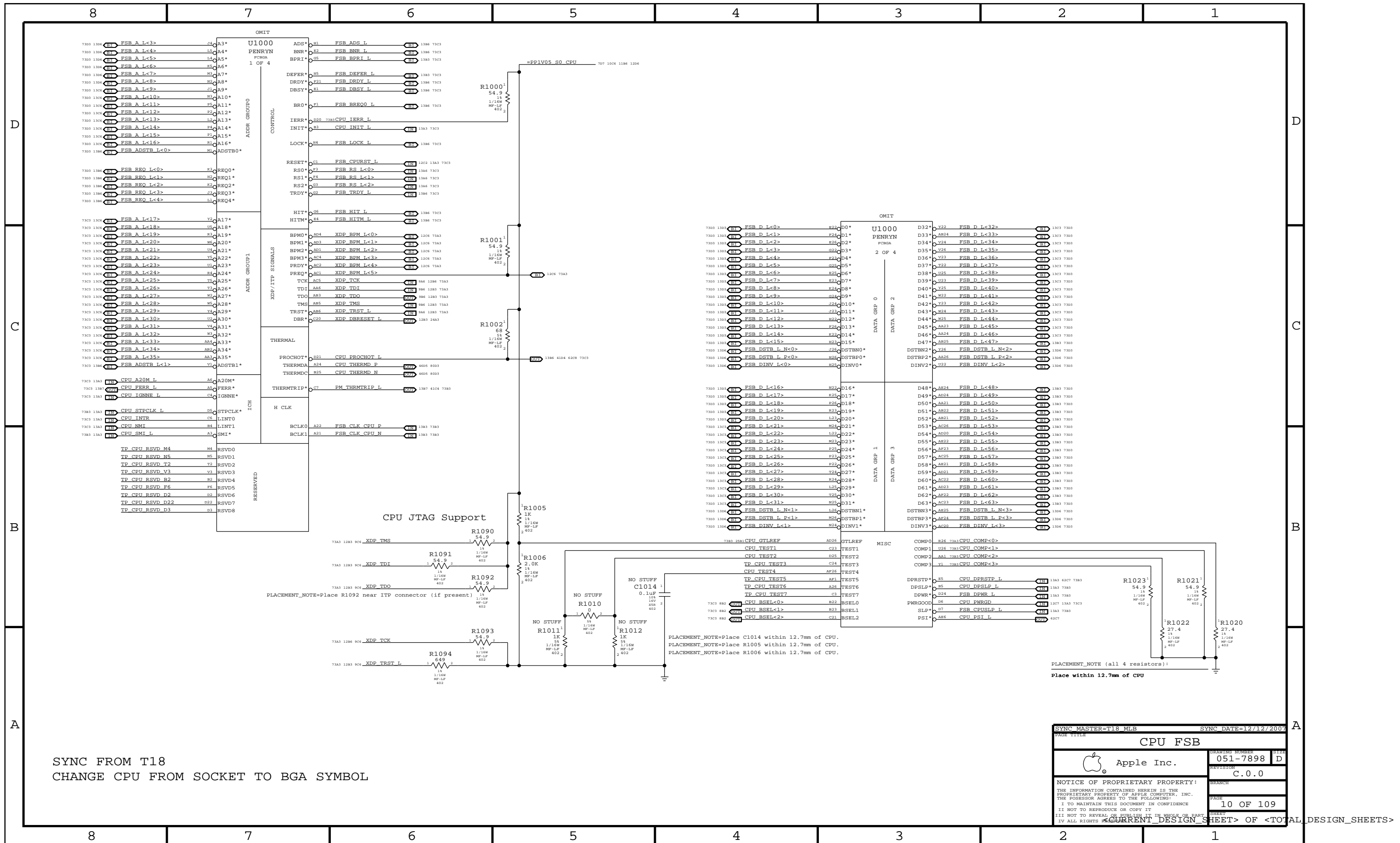
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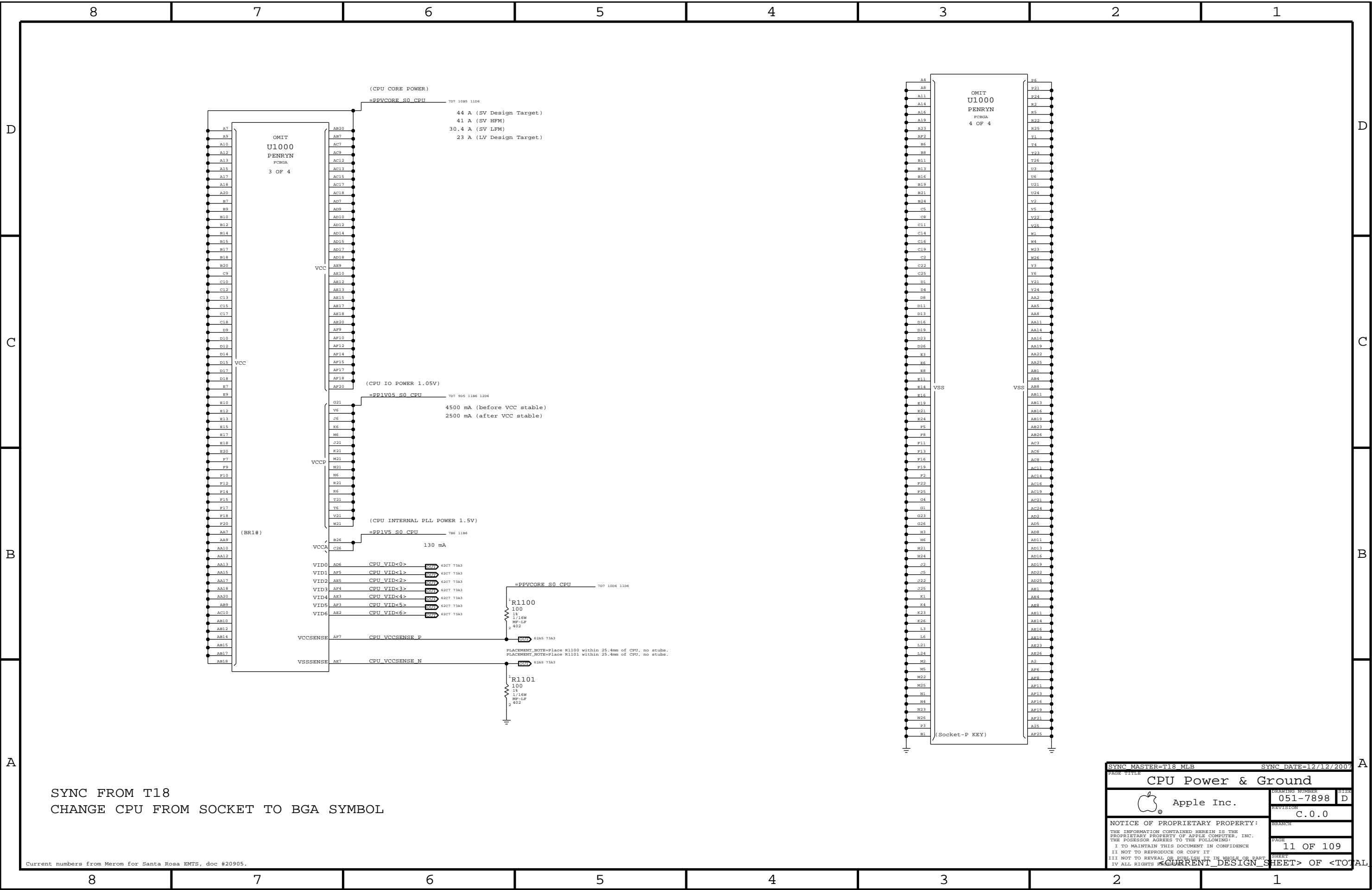
[illegible]


8	7	6	5	4	3	2	1
Functional Test Points							
D	Fan Connectors (NEED 3 TP)		RIGHT CLUTCH CONN		DEBUG VOLTAGE		
	MIC FUNC_TEST						
	SPEAKER FUNC_TEST						
	THERMAL FUNC_TEST						
	LVDS FUNC_TEST						
C							
B							
A							

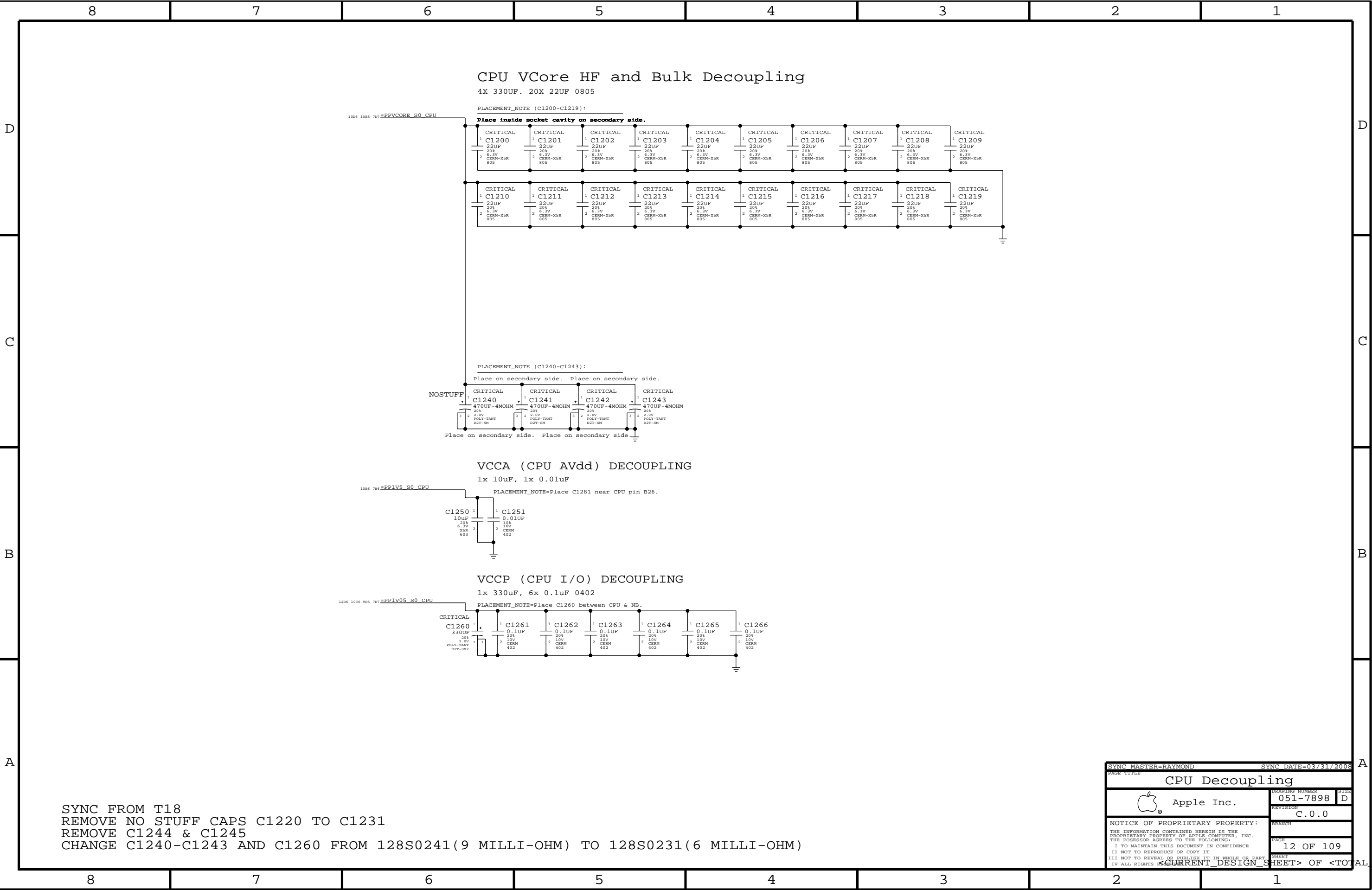








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CPU Power & Ground			
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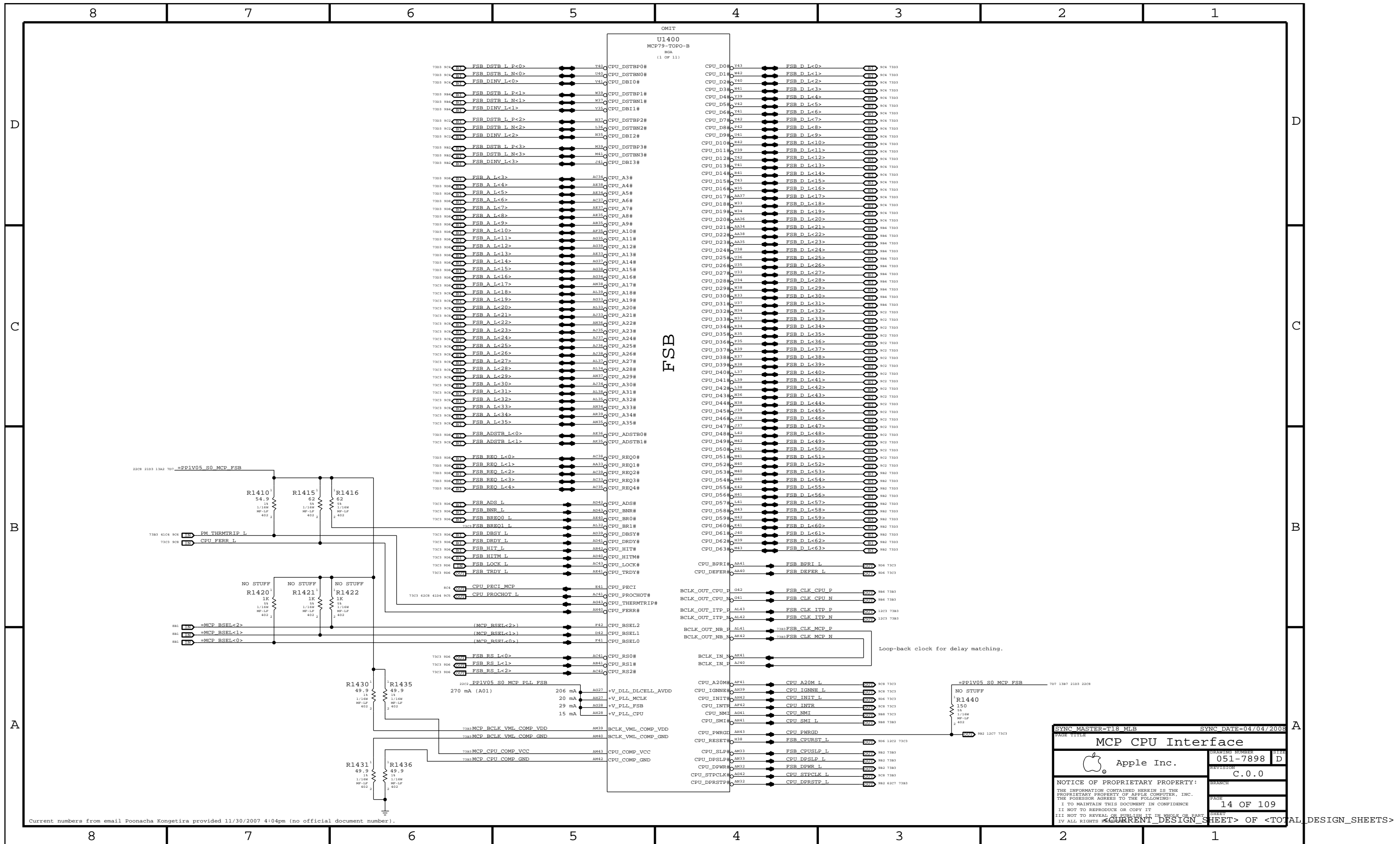
C

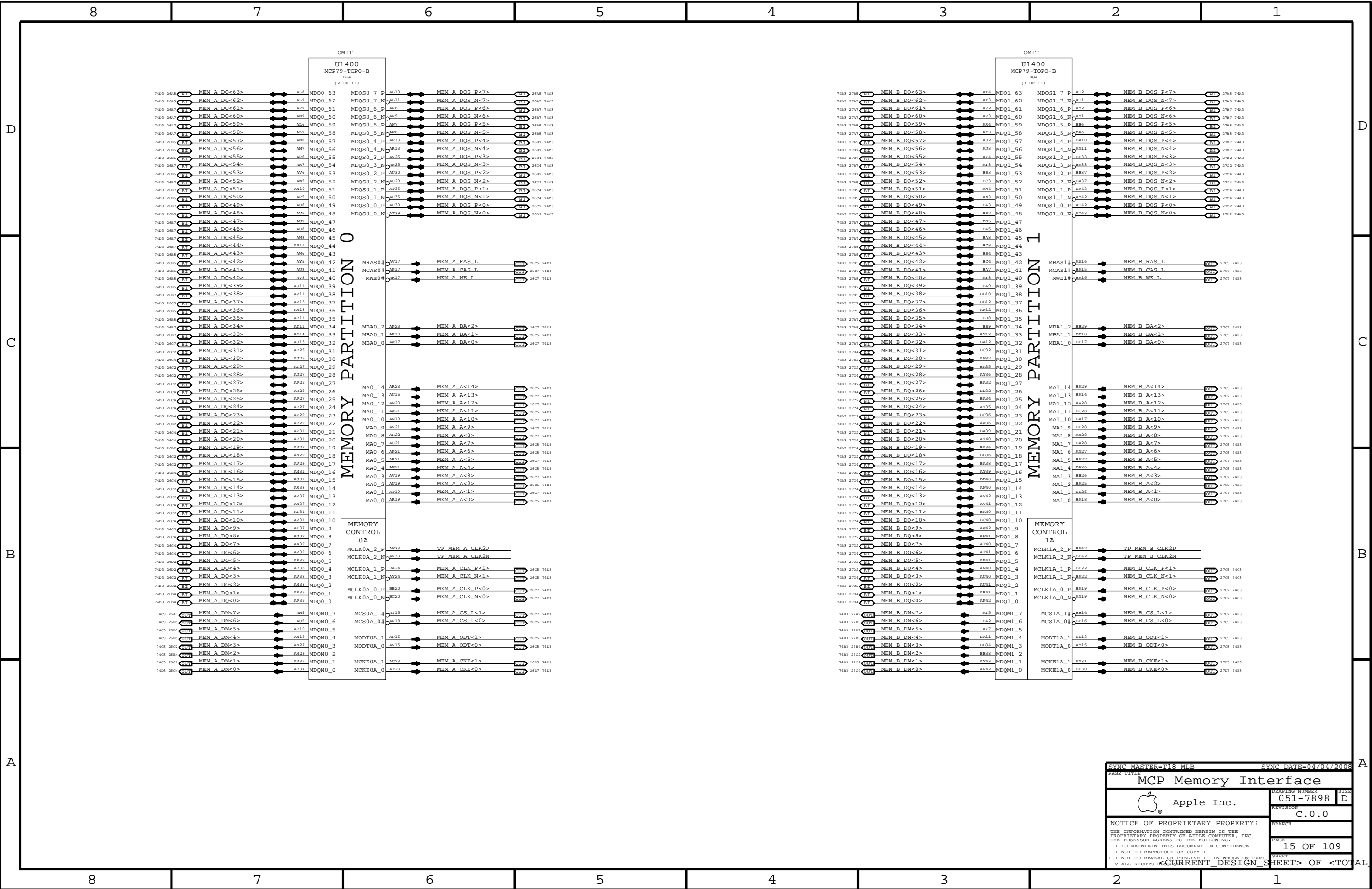


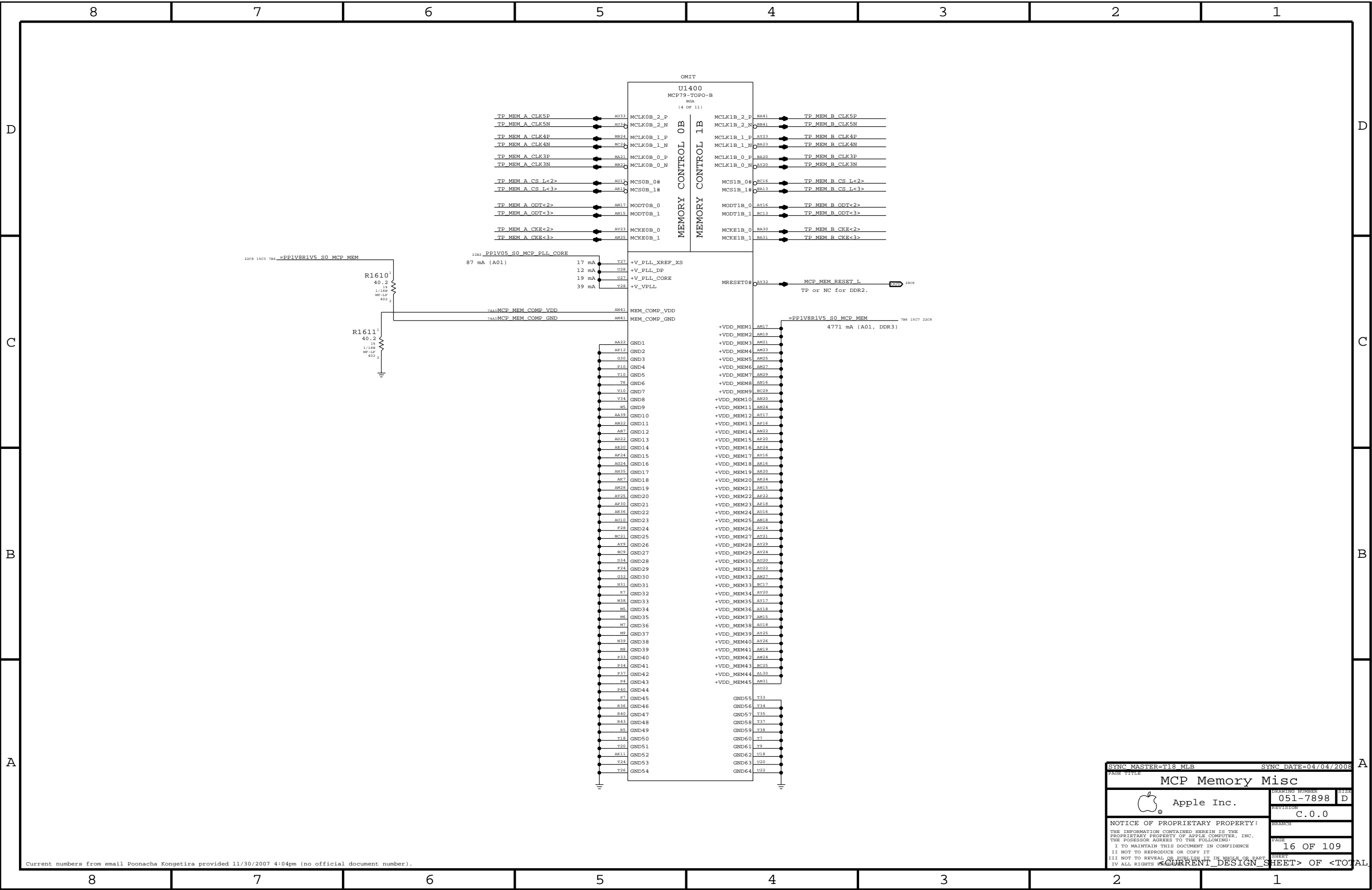
B

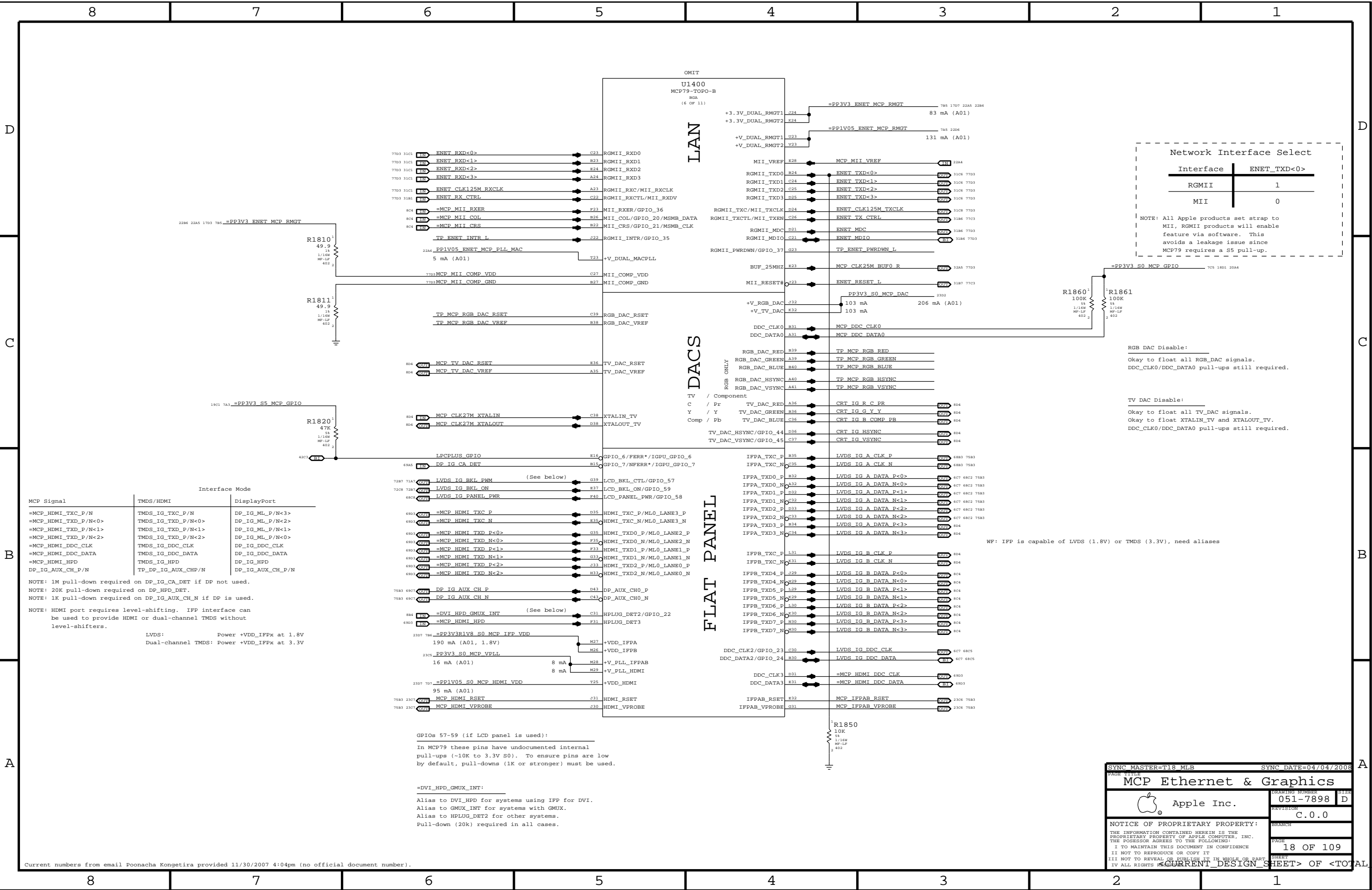
B

A









Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

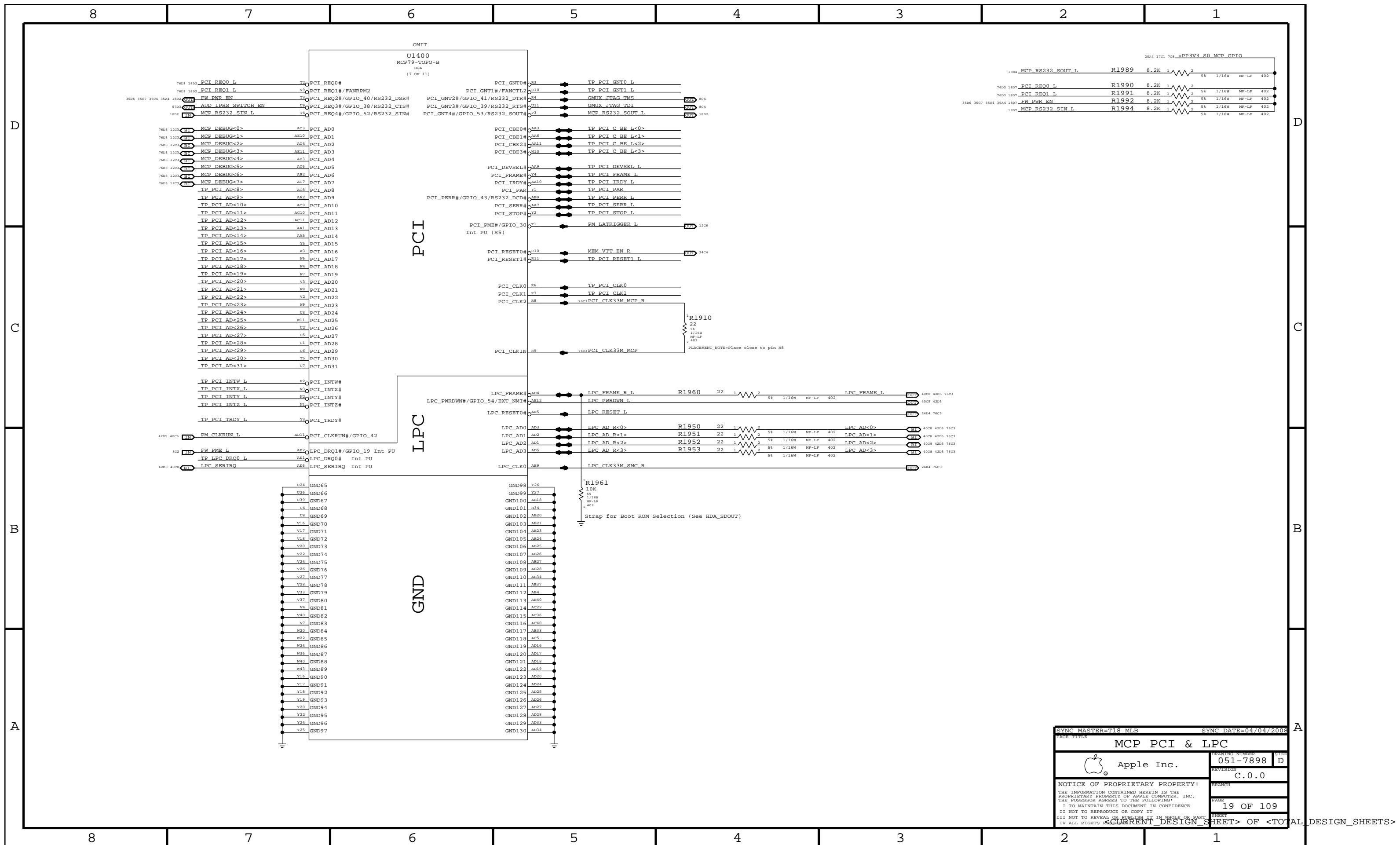
NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

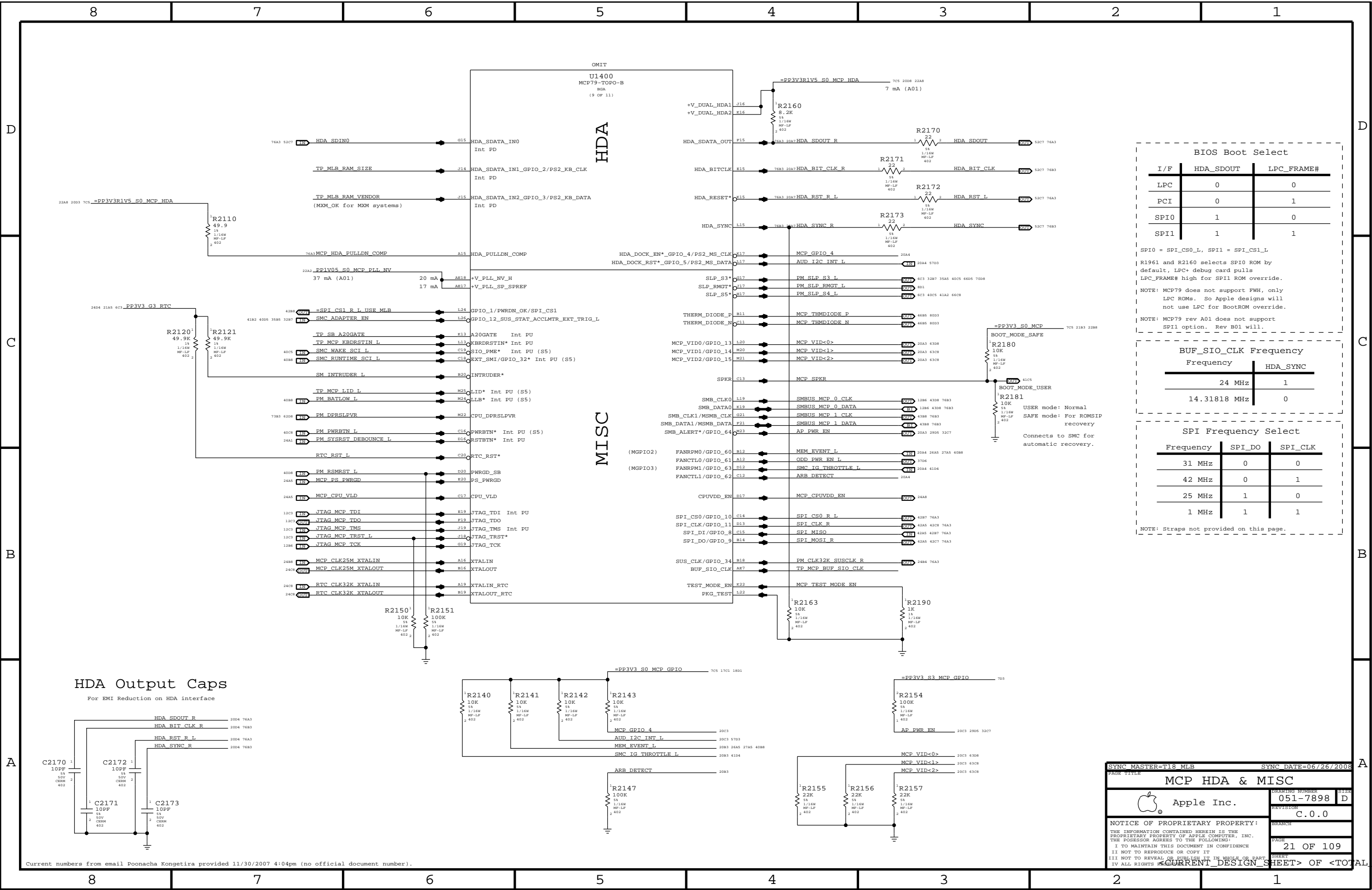
TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

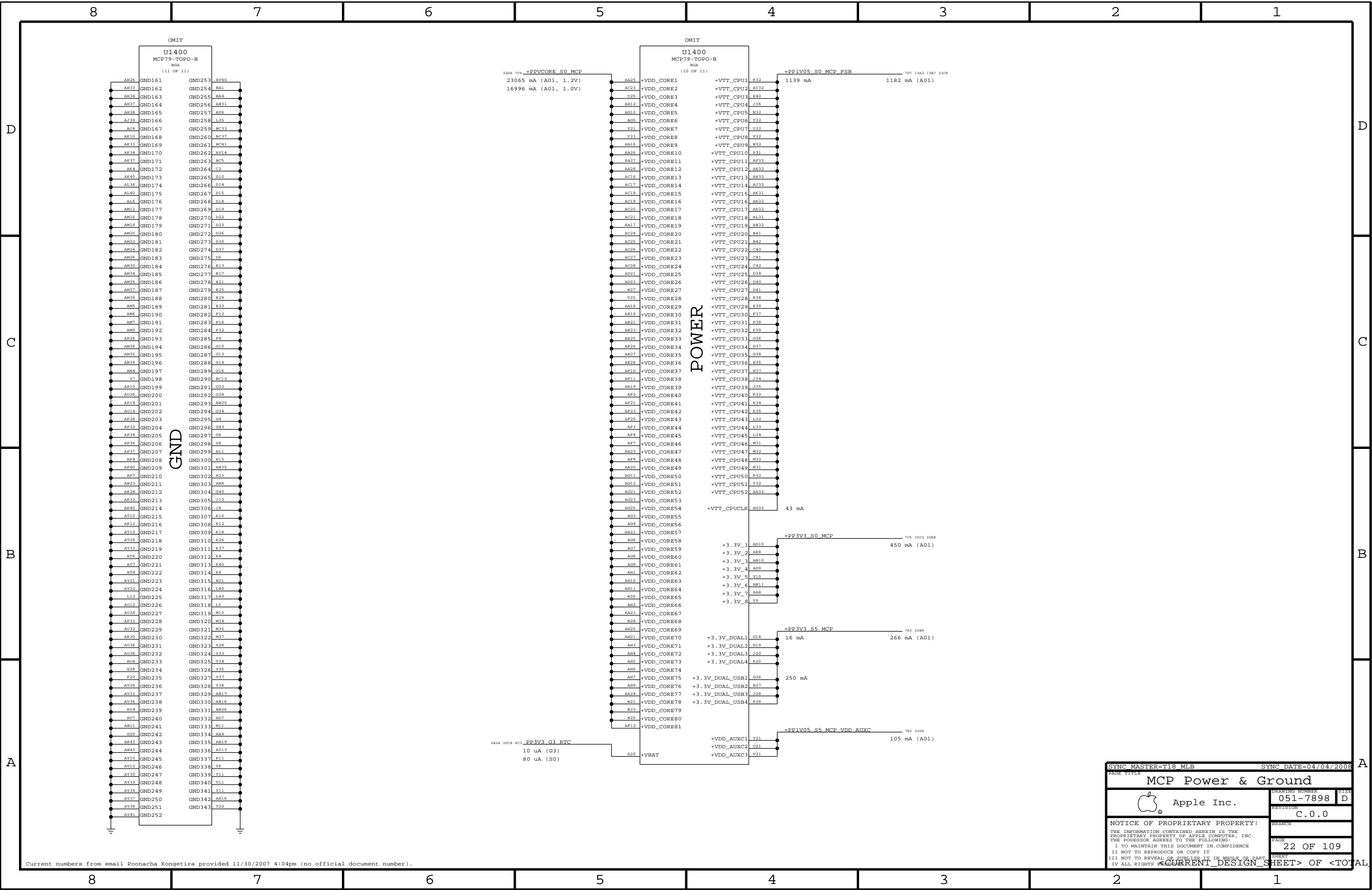
WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

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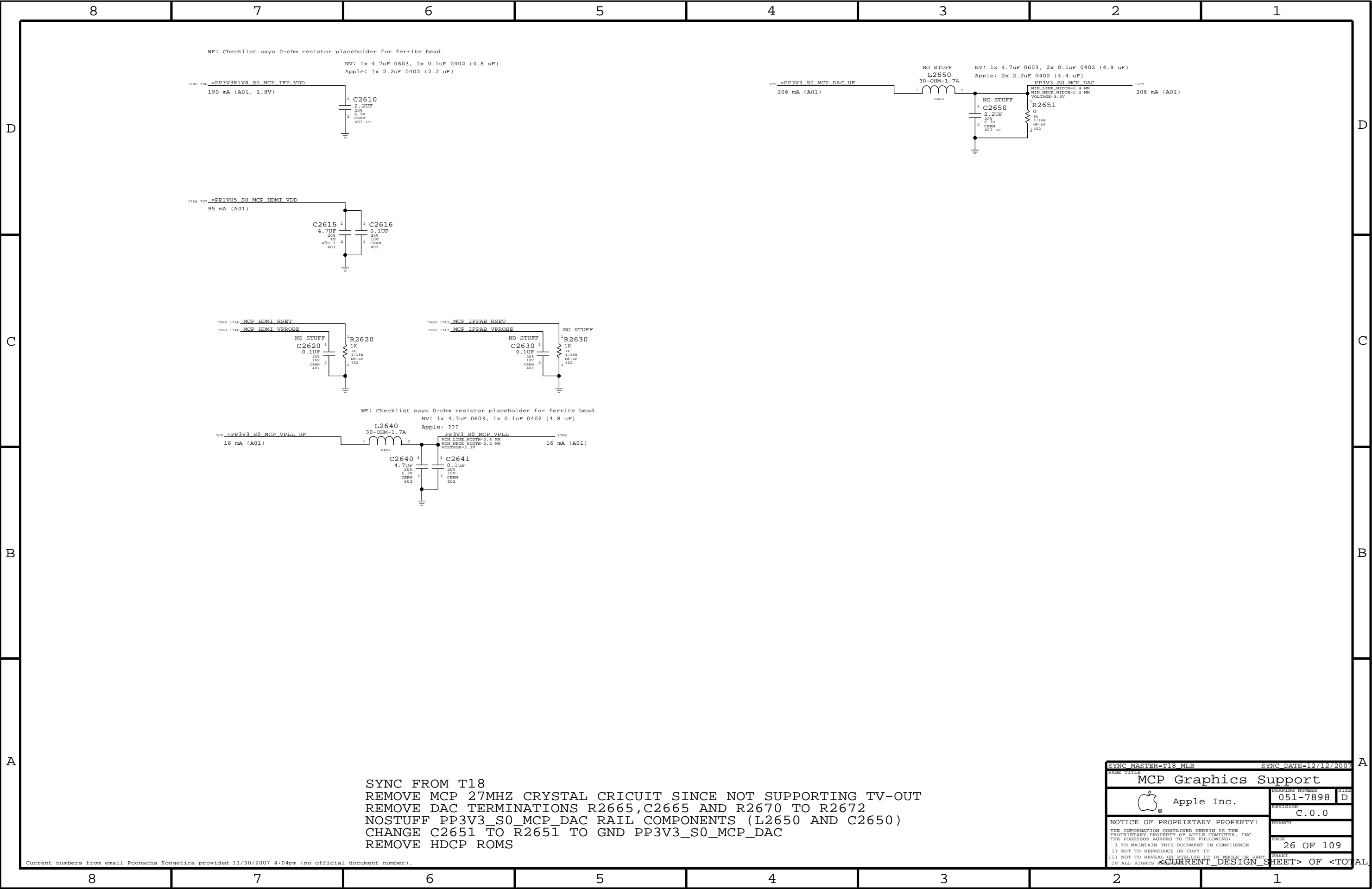







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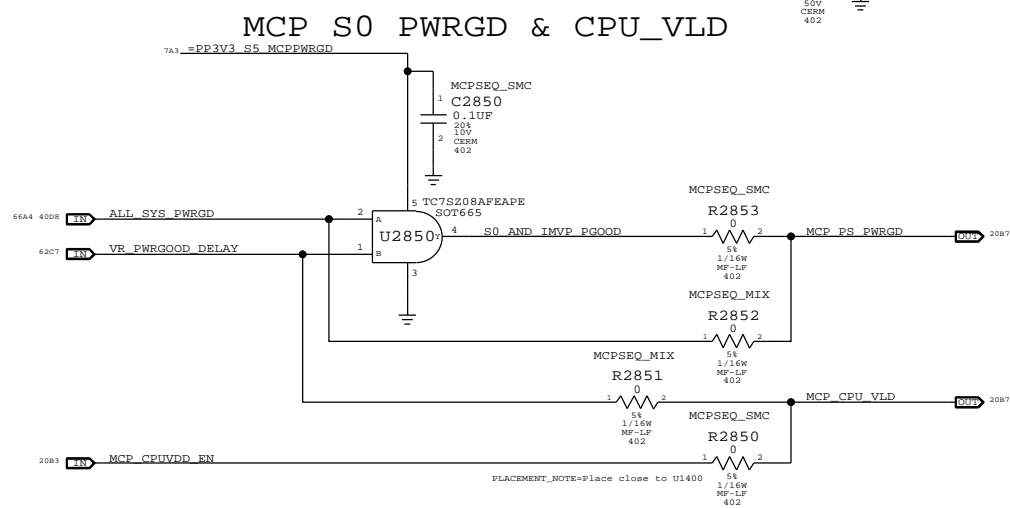
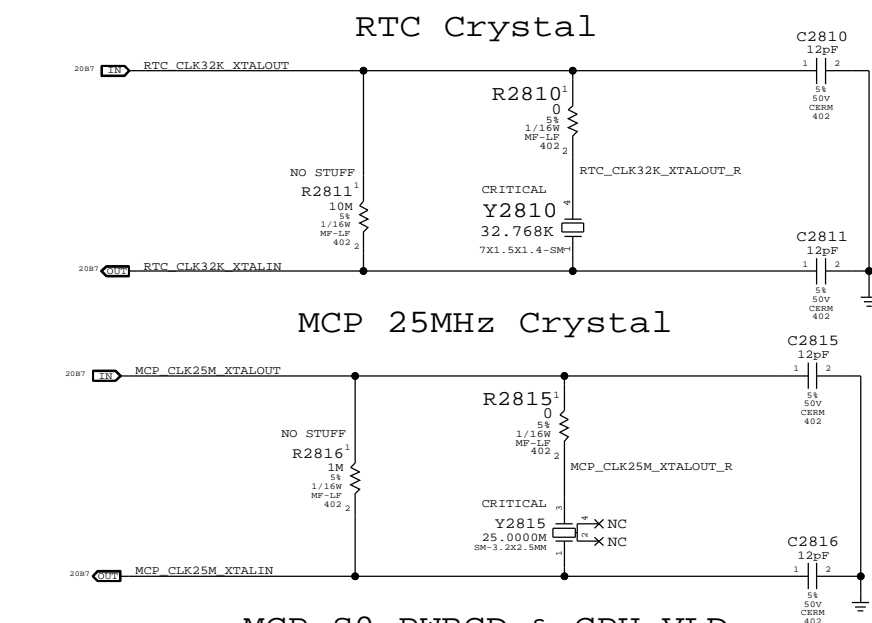
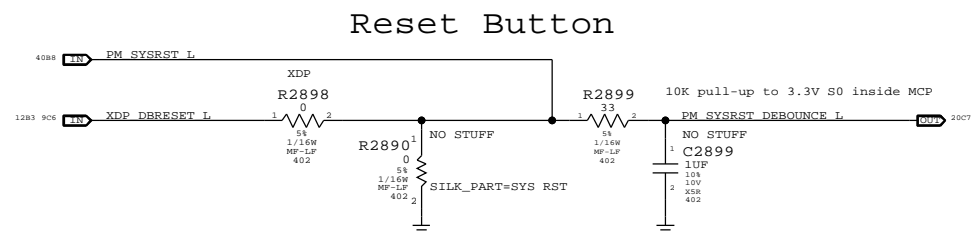
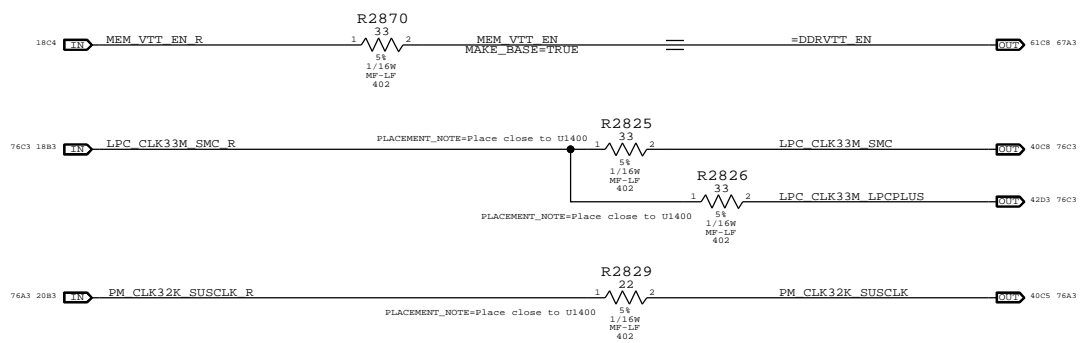
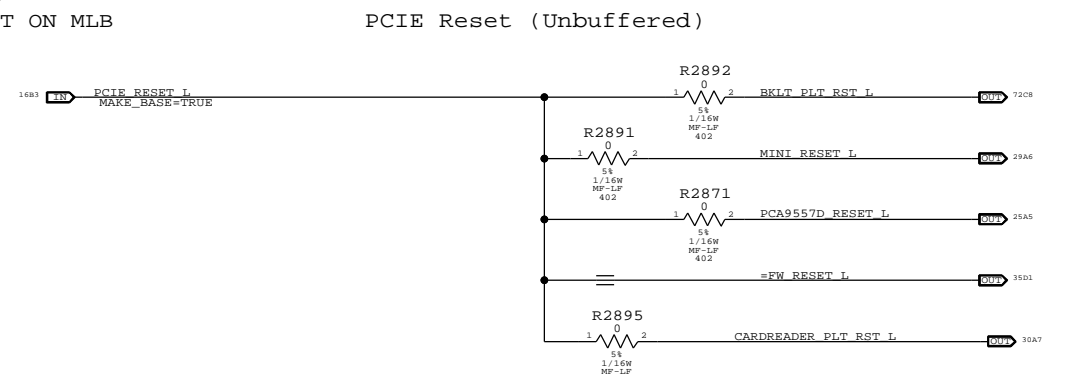
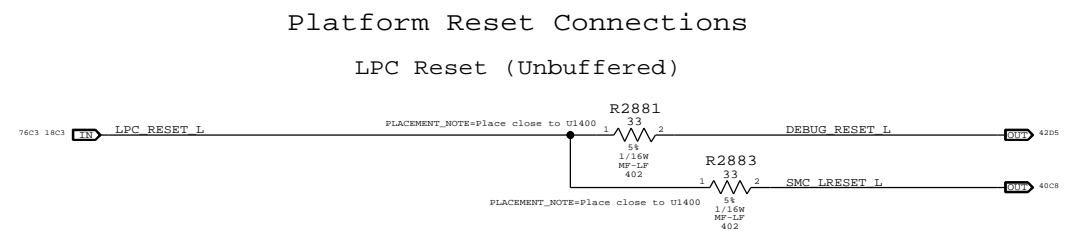
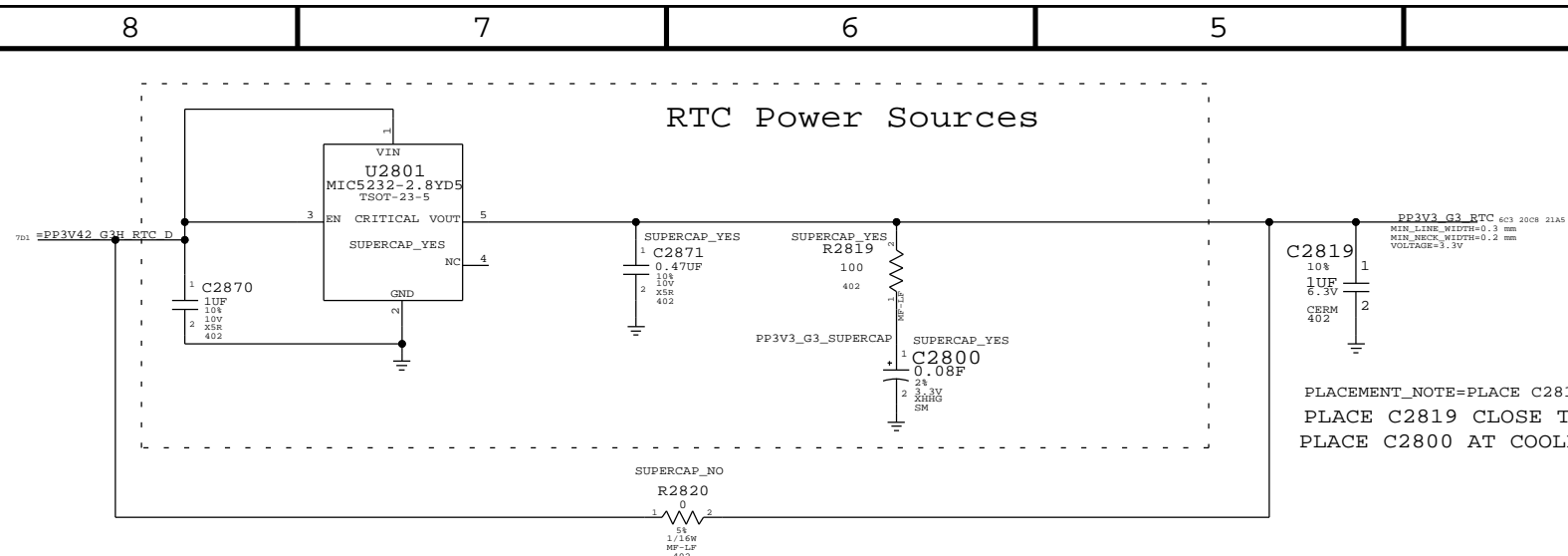
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SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC
REMOVE HDCP ROMS

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MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_FWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).


NOTE: if CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

```

SYNC FROM T18
CHANGE RESET BUTTON TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

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SYNC MASTER-RAYMOND		SYNC DATE=04/05/2008	
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SB Misc			
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Page Notes

Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:

- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

VREFMRGN
NO_VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ

MEM A VREF CA

MEM B VREF DQ

MEM B VREF CA

CPU FSB VREF

A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

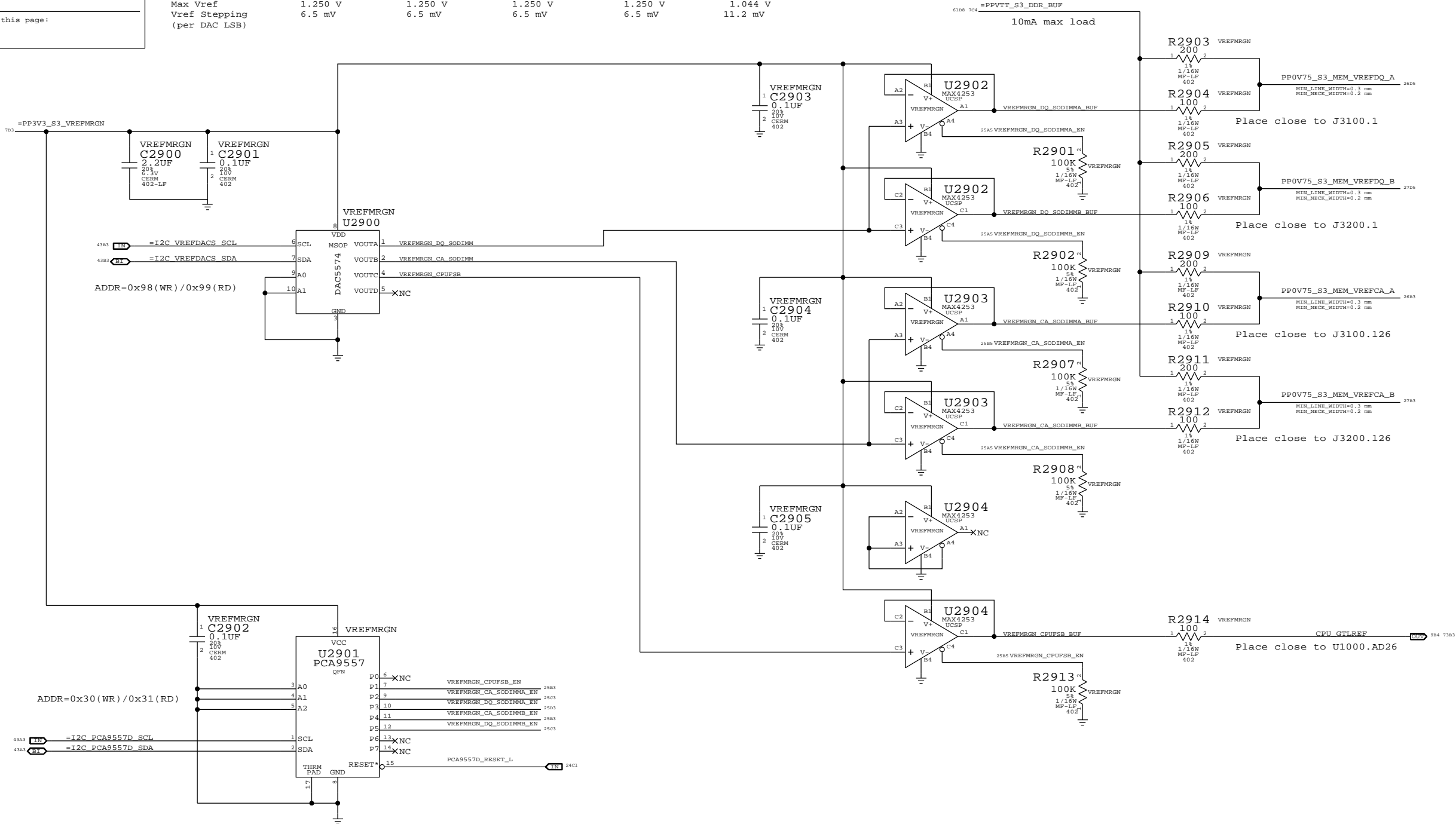
B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

A
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

B
0x00
0x87
-3.75 mA
5 mA
0.75 V
0.375 V
1.250 V
6.5 mV

C
0x00
0x55
-0.91 mA
0.52 mA
0.70 V
0.091 V
1.044 V
11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0.5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC MASTER=BEN SYNC DATE=03/31/2008

FSB/DDR3 Vref Margining

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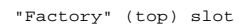
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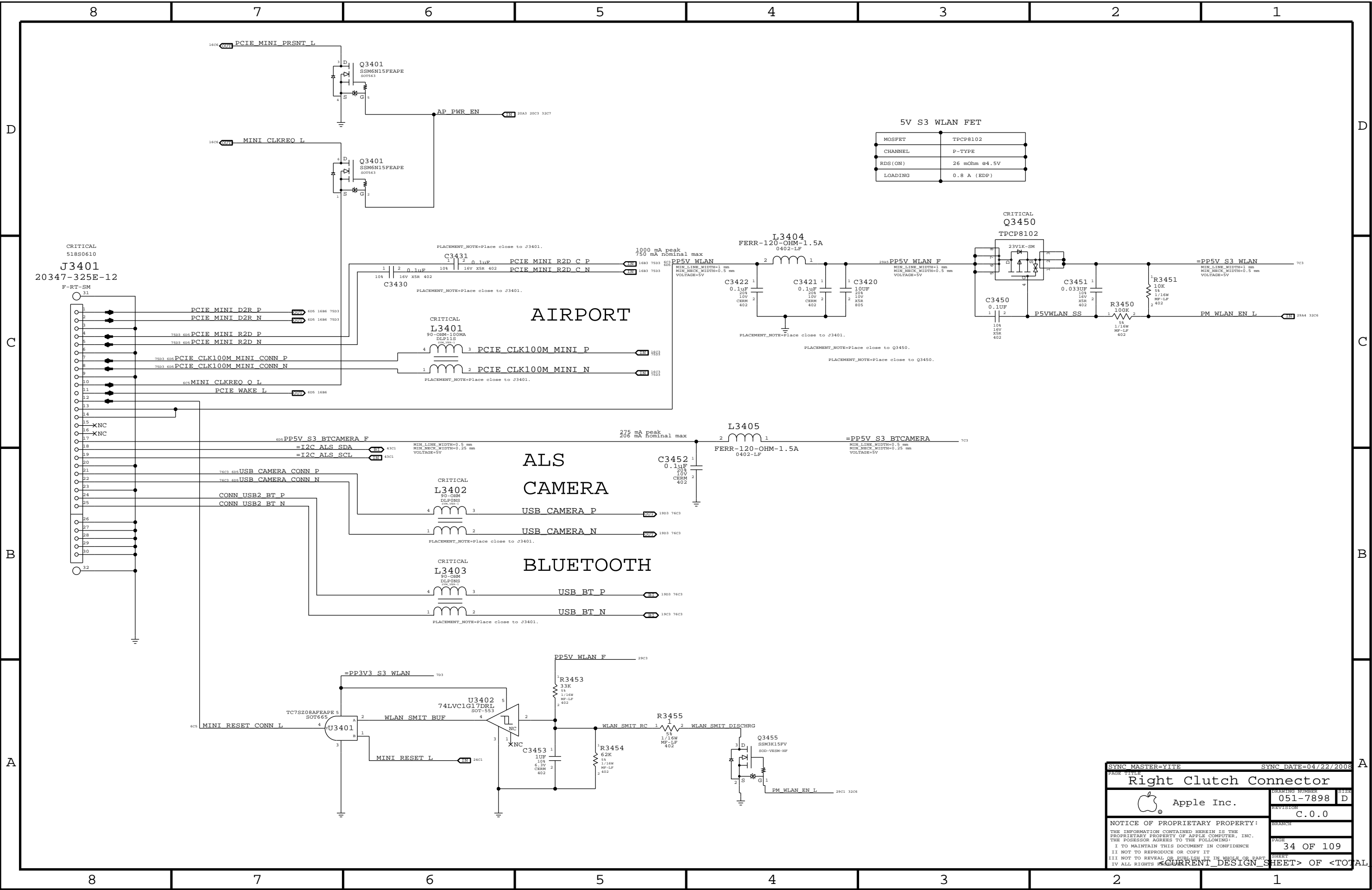
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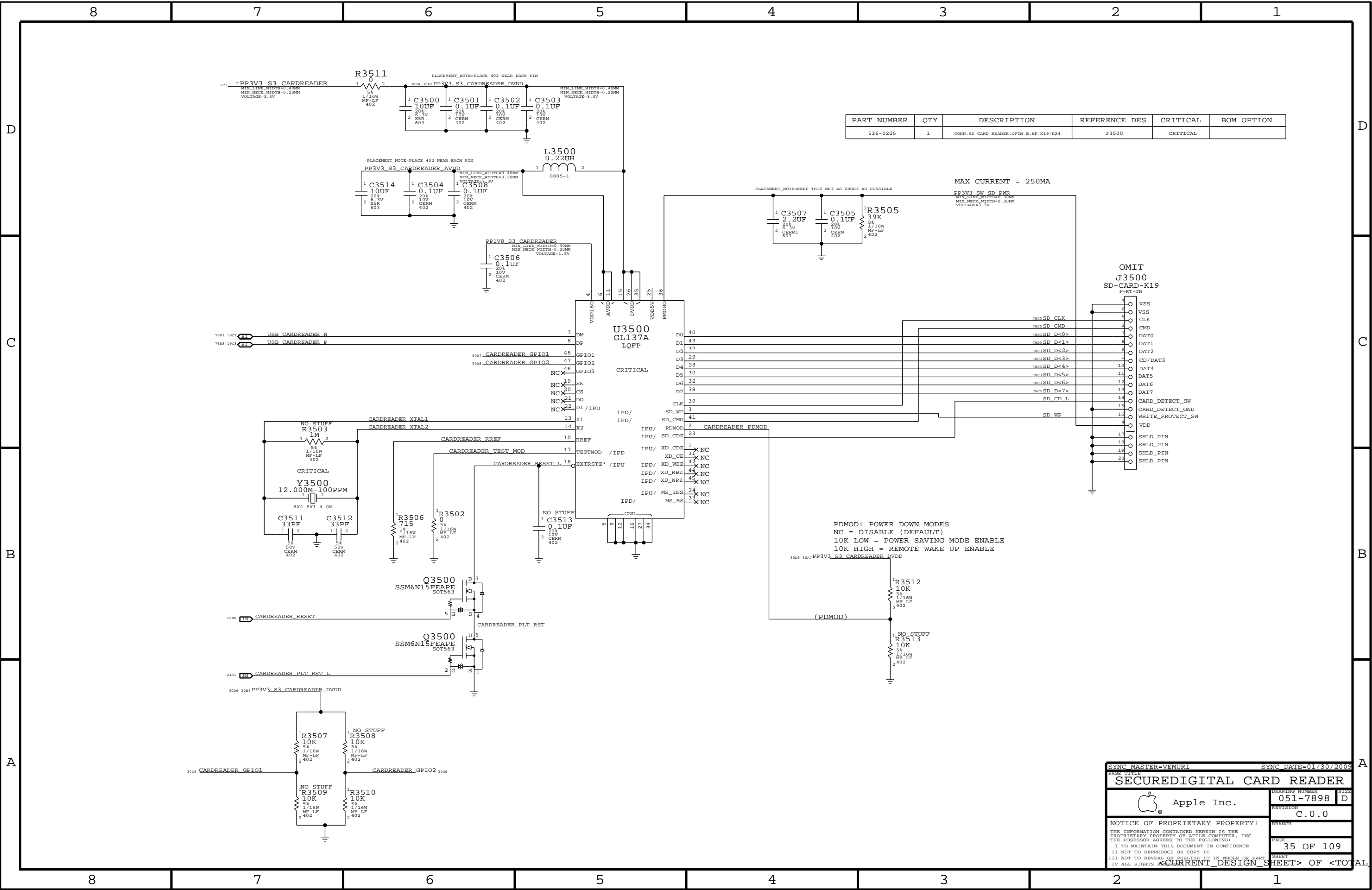
CURRENT DESIGN SHEET OF TOTAL DESIGN SHEETS

BOM options provided by this page:
(NONE)




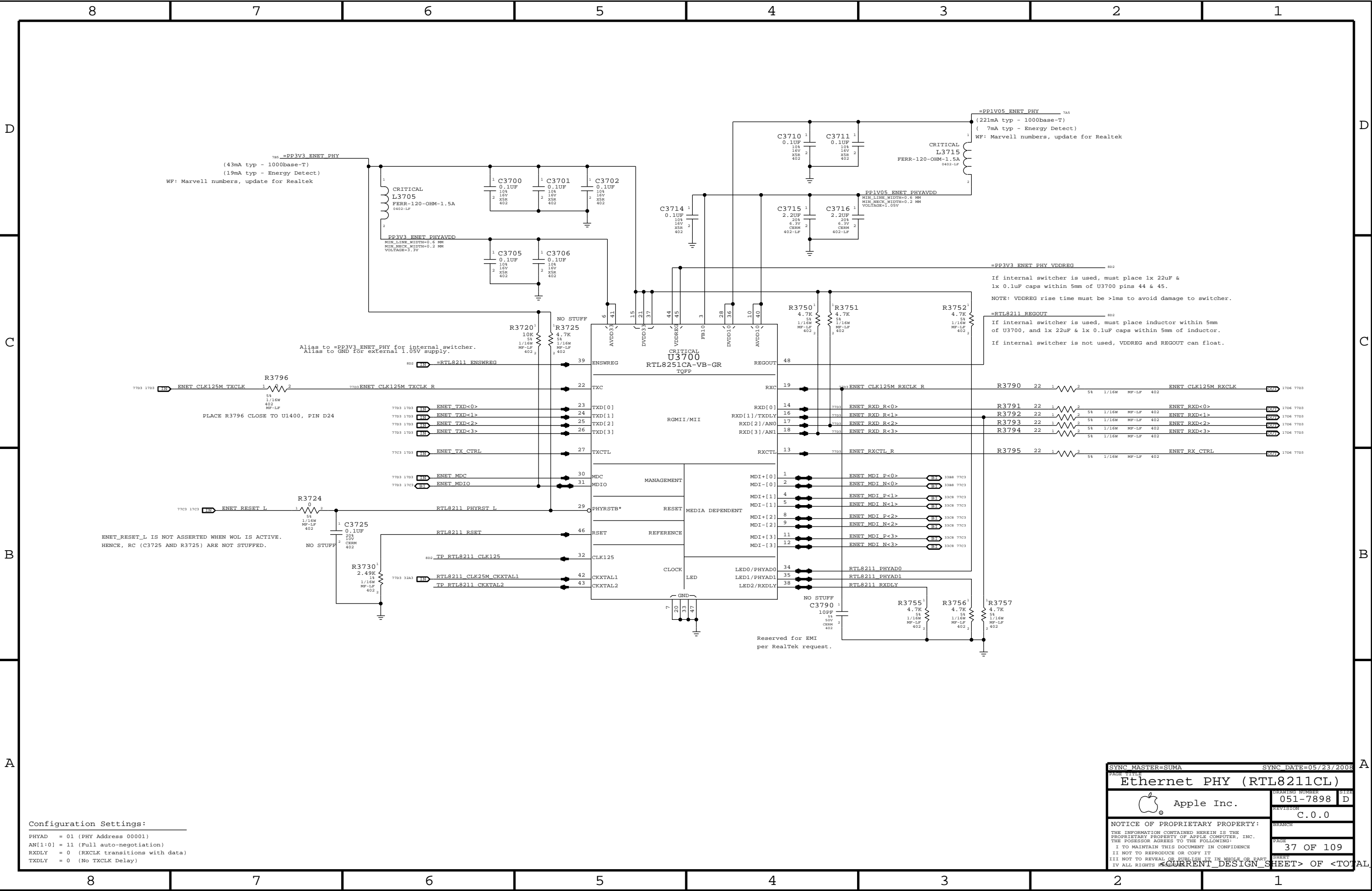
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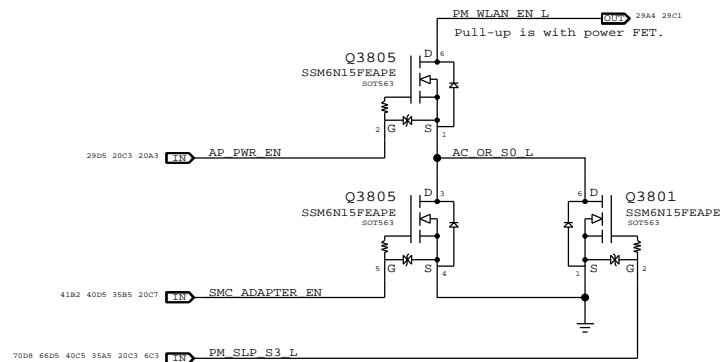
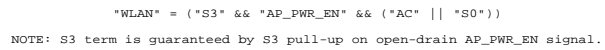




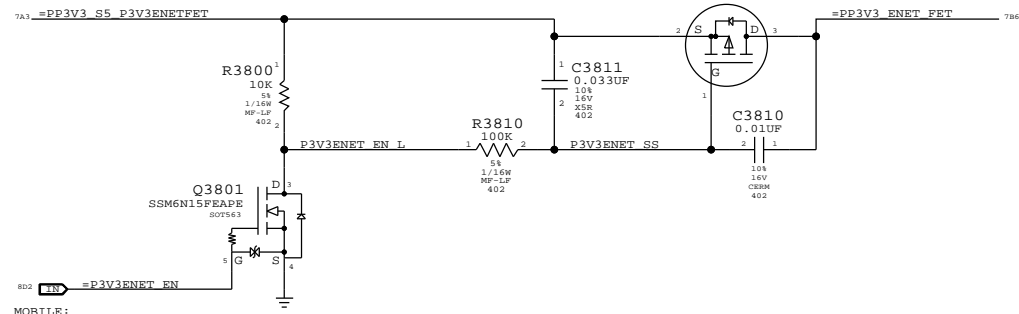
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B,HF,K19/K24	J3500	CRITICAL	

SYNC MASTER=VEMURI		SYNC DATE=01/30/2009	
PAGE TITLE			
SECUREDIGITAL CARD READER			
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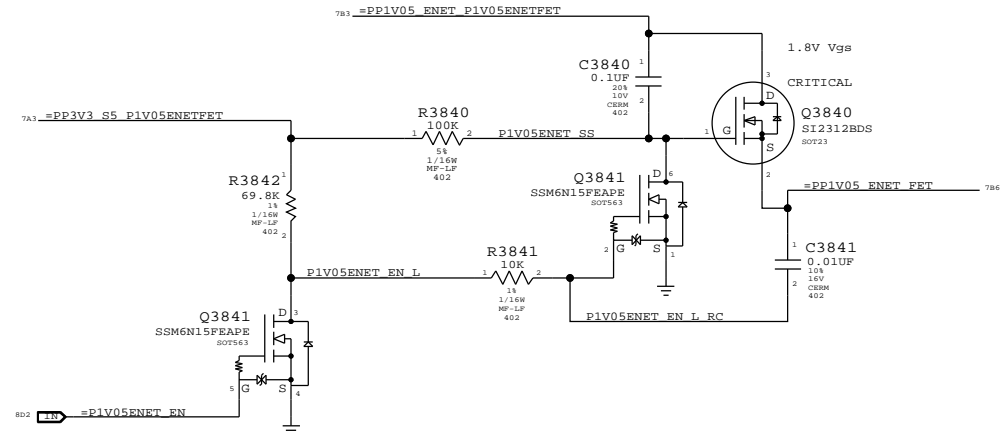


@ 2.5V Vgs:	CRITICAL
Rds(on) = 90mOhm max	Q3810
I(max) = 1.7A (85C)	NTR4101P



Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

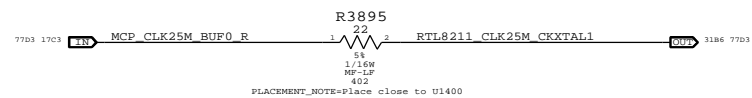
7b3 `=PP1V05 ENET P1V05ENETFET` 1.8V Vgs




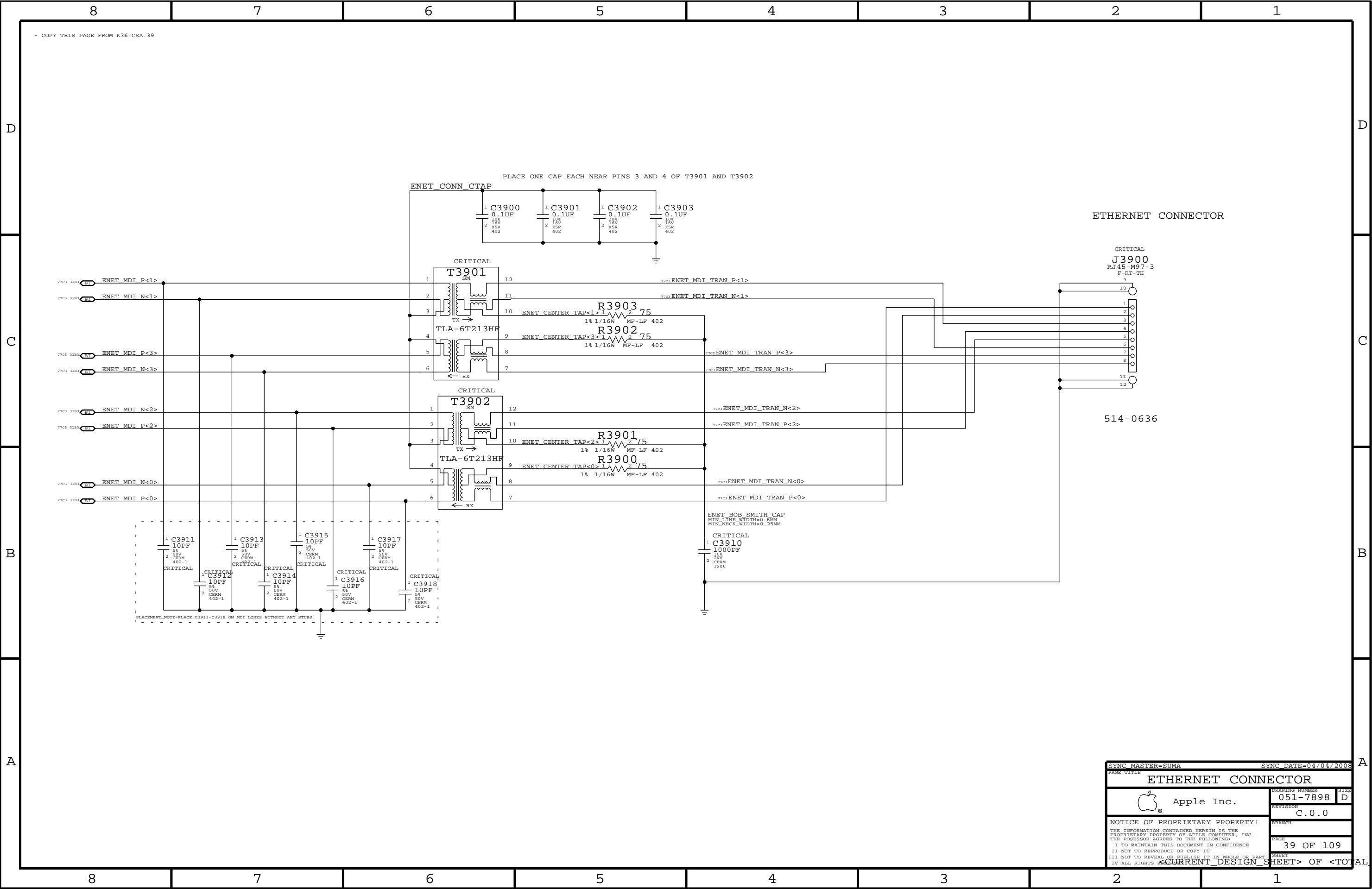
Non-ARB:


Recommend aliasing PM_SLP_RMGT_L and
=P1V05ENET_EN. Nets separated on
ARB for alternate power options.

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



SYNCH MASTER-SUMA		SYNCH DATE=07/01/2008	
FORM 1-7-84			
Ethernet & AirPort Support			
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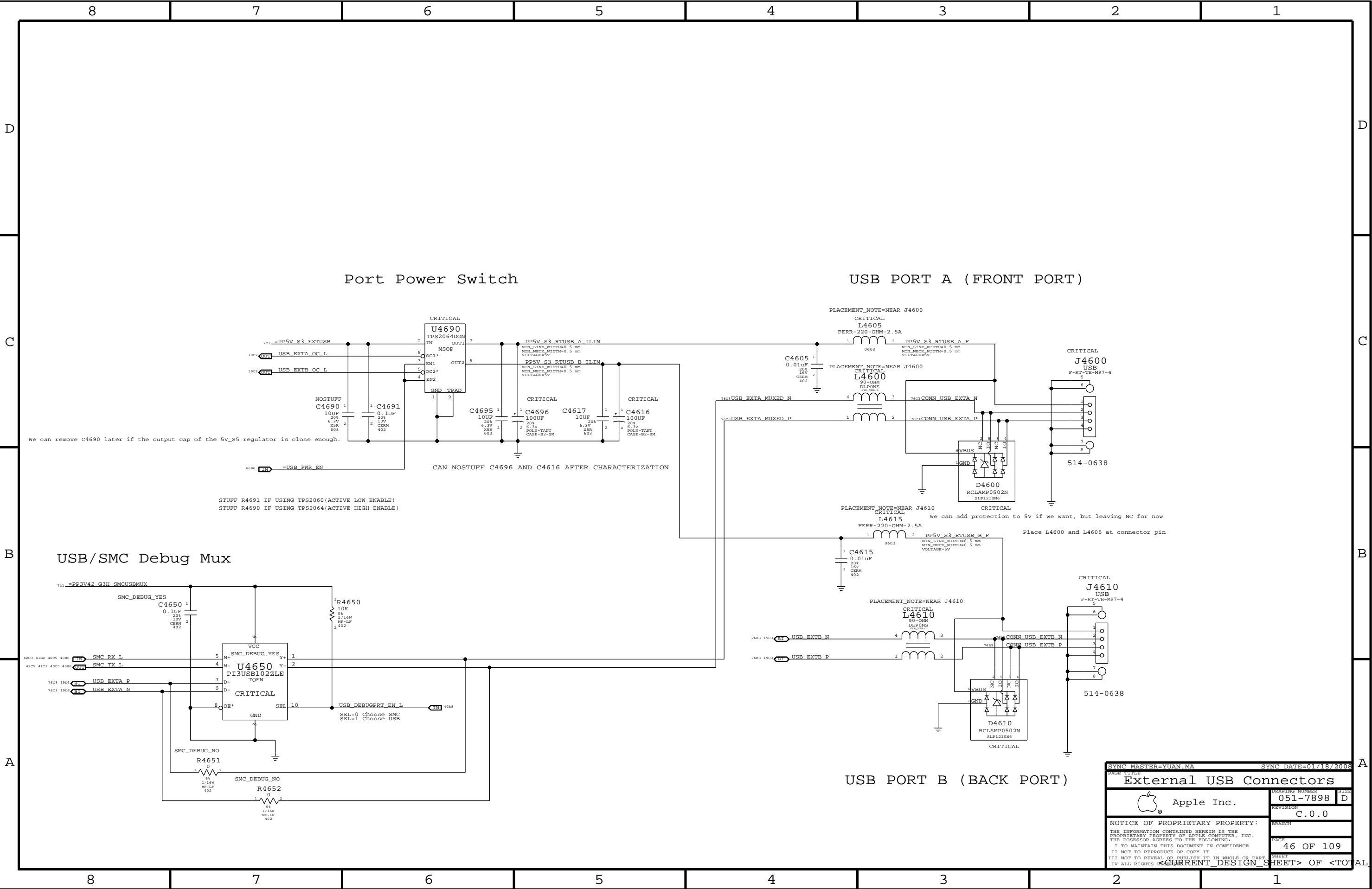
A

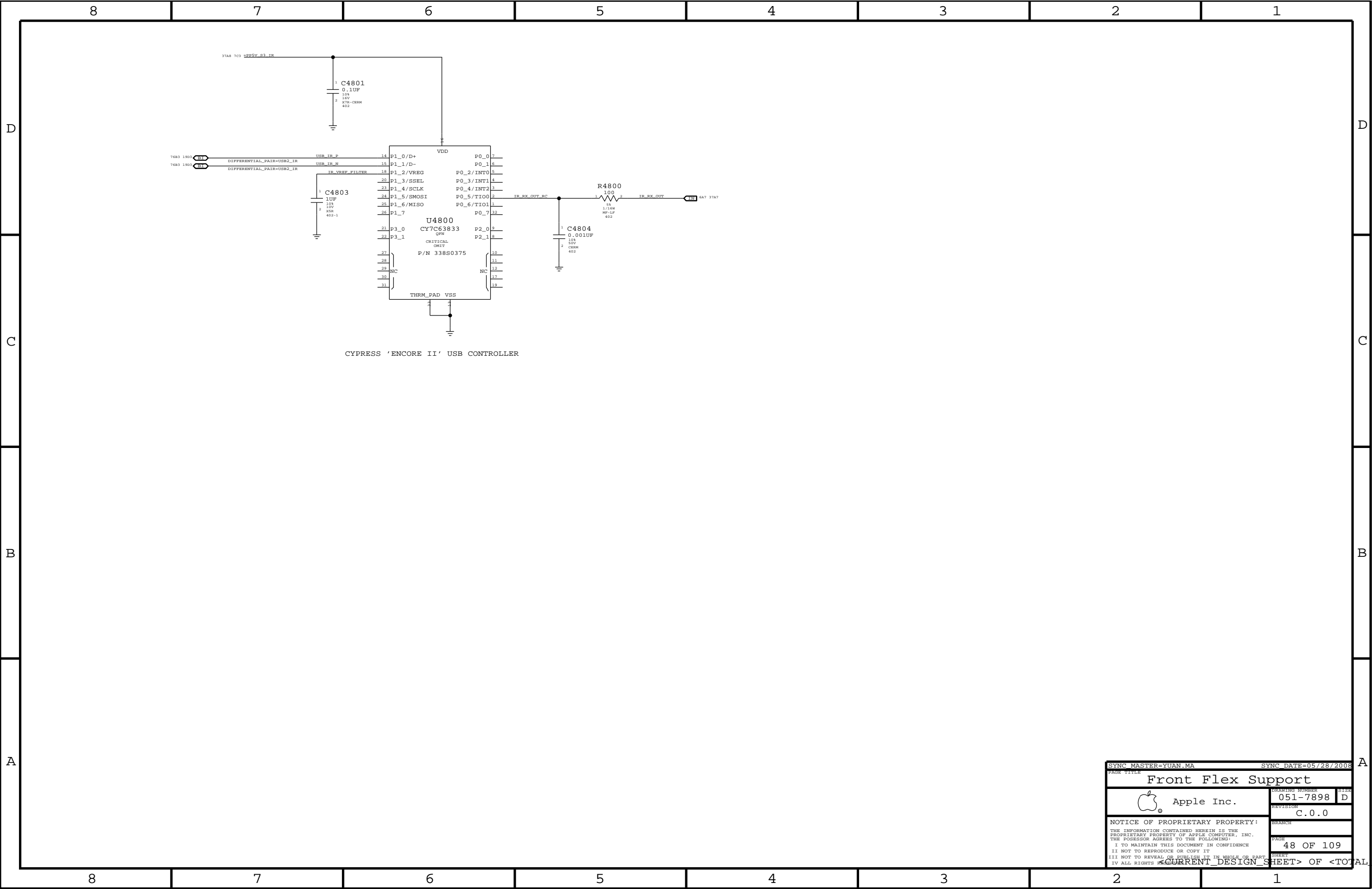


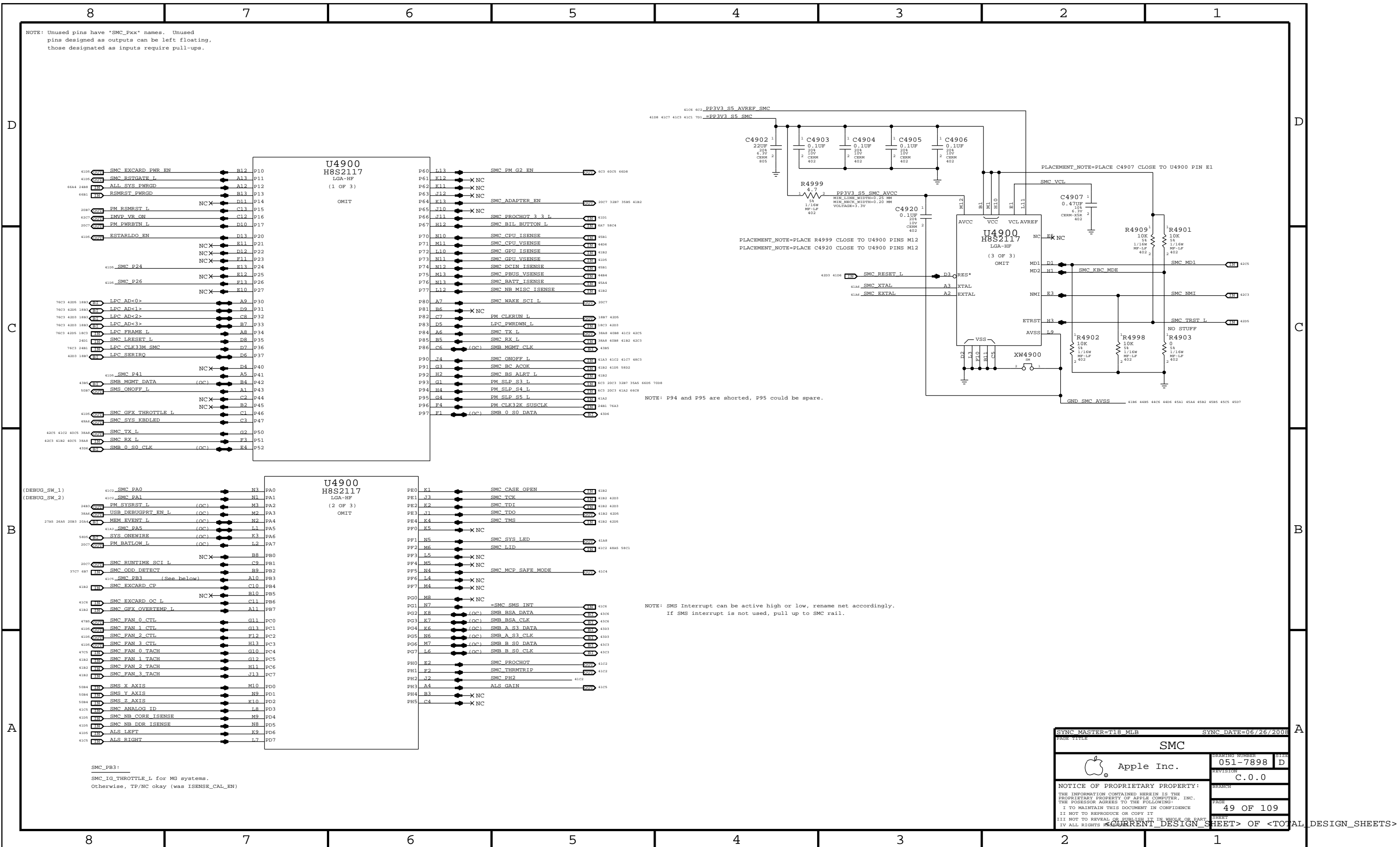
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CRITICAL
LPCPLUS
J5100
55909-0374
M-ST-SM

42C8 42C7 7D1 =PP3V3 S5 LPCPLUS
7D5 =PP5V S0 LPCPLUS

42C8 42C7 7D1 =PP3V3 S5 LPCPLUS
7D5 =PP5V S0 LPCPLUS

76C3 40C8 18B3 LPC AD<0>
76C3 40C8 18B3 LPC AD<1>

76A3 42C5 SPI ALT MOSI
76A3 42B8 SPI ALT MISO
76C3 40C8 18C3 LPC FRAME L
40C5 18B7 PM CLKRUN L
41B2 40B8 SMC TMS
SMC TDO
SMC TRST L
40C1 SMC MD1
40C3 SMC MD1
41C2 40C5 40B8 38A8 SMC TX L

1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
21 22
23 24
25 26
27 28
29 30
33 34

LPC CLK33M LPCPLUS
LPC AD<2>
LPC AD<3>
SPIROM USE M1B
SPI ALT CLK
SPI ALT CS L
LPC SERIRQ
LPC PWRDWN L
SMC TDI
SMC TCK
SMC RESET L
SMC NMI
SMC RX L
LPCPLUS GPIO

24H1 76C3
18B3 40C8 76C3
42B7
42C5 76A3
42B5
18B7 40C8
18C3 40C5
40B5 41B3
40C3 41B2
40C1
38A8 40B8 40C5 41B3
17B7

516S0573

Diagram illustrating the SPI interface connections for the U5110 and U5120 chips, showing the connection of the SPI bus (CLK, MOSI, MISO, CS) to the U5110 and U5120 chips.

U5110 Connections:

- SEL:** 10
- OE*:** 8
- VCC:** 1
- GND:** 2
- Y+:** 1
- Y-:** 2
- M+:** 4
- M-:** 5
- D+:** 7
- D-:** 6

U5120 Connections:

- SEL:** 10
- OE*:** 8
- VCC:** 1
- GND:** 2
- Y+:** 1
- Y-:** 2
- M+:** 4
- M-:** 5
- D+:** 7
- D-:** 6

Resistors:

- R5190:** 10K, 5%, 1/16W, MF, LE, 402, 2
- R5191:** 10K, 5%, 1/16W, MF, LE, 402, 2
- R5140:** 100K, 5%, 1/16W, MF, LE, 402, 2
- R5146:** 0, 5%, 1/16W, MF, LE, 402, 2
- R5144:** 20K, 5%, 1/16W, MF, LE, 402, 2


Capacitors:

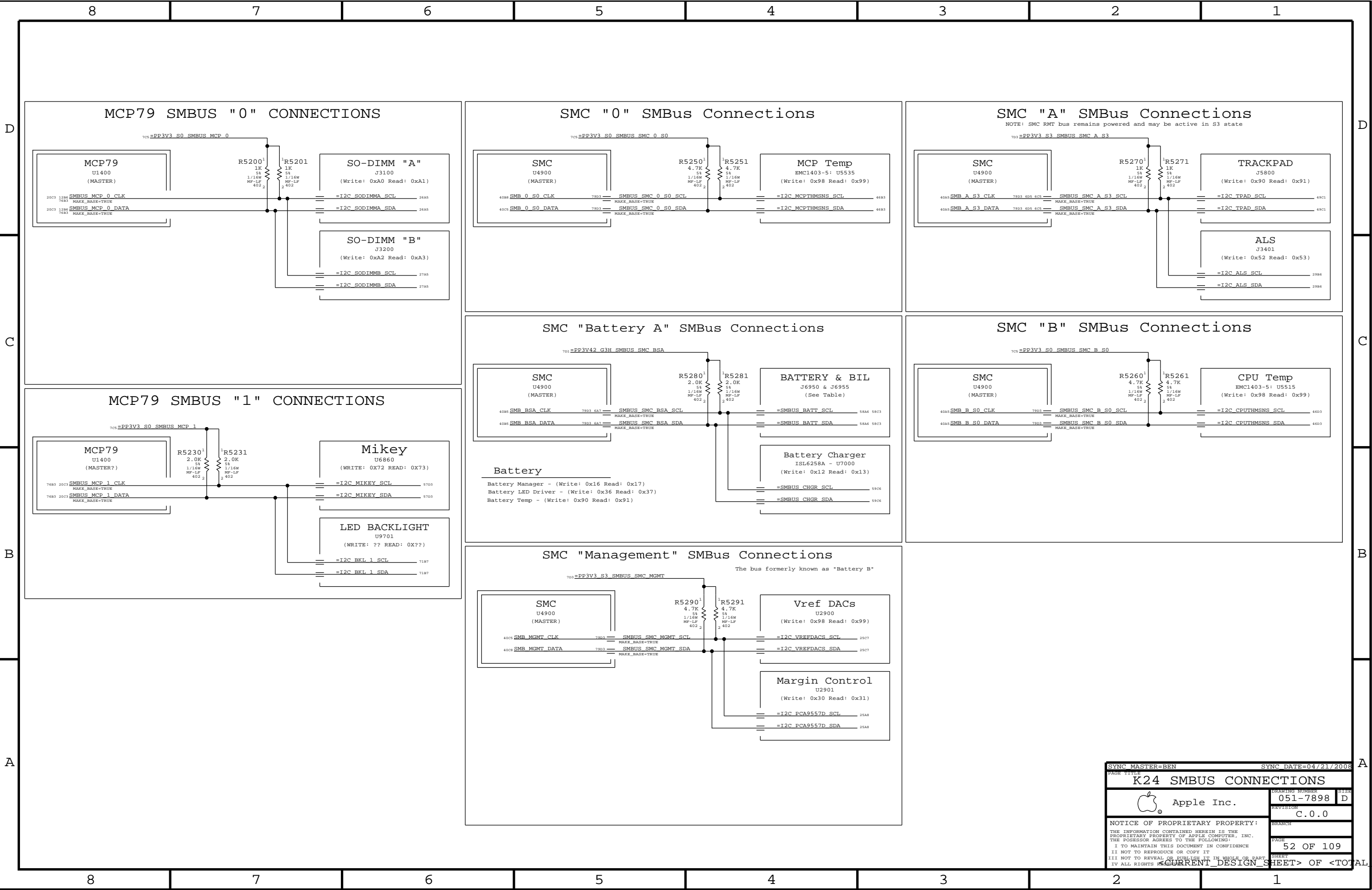
- C5114:** 0.1uF, 20V, 10V, CERM, 402
- C5124:** 0.1uF, 20V, 10V, CERM, 402

Labels:

- SEL HIGH OUTPUTS TO D (ON BOARD ROM)**
- SEL LOW OUTPUTS TO M (FRANKCARD ROM)**
- Pull-up on debug card**
- PLACEMENT_NOTE=PLACE NEXT TO U1400**

[illegible]

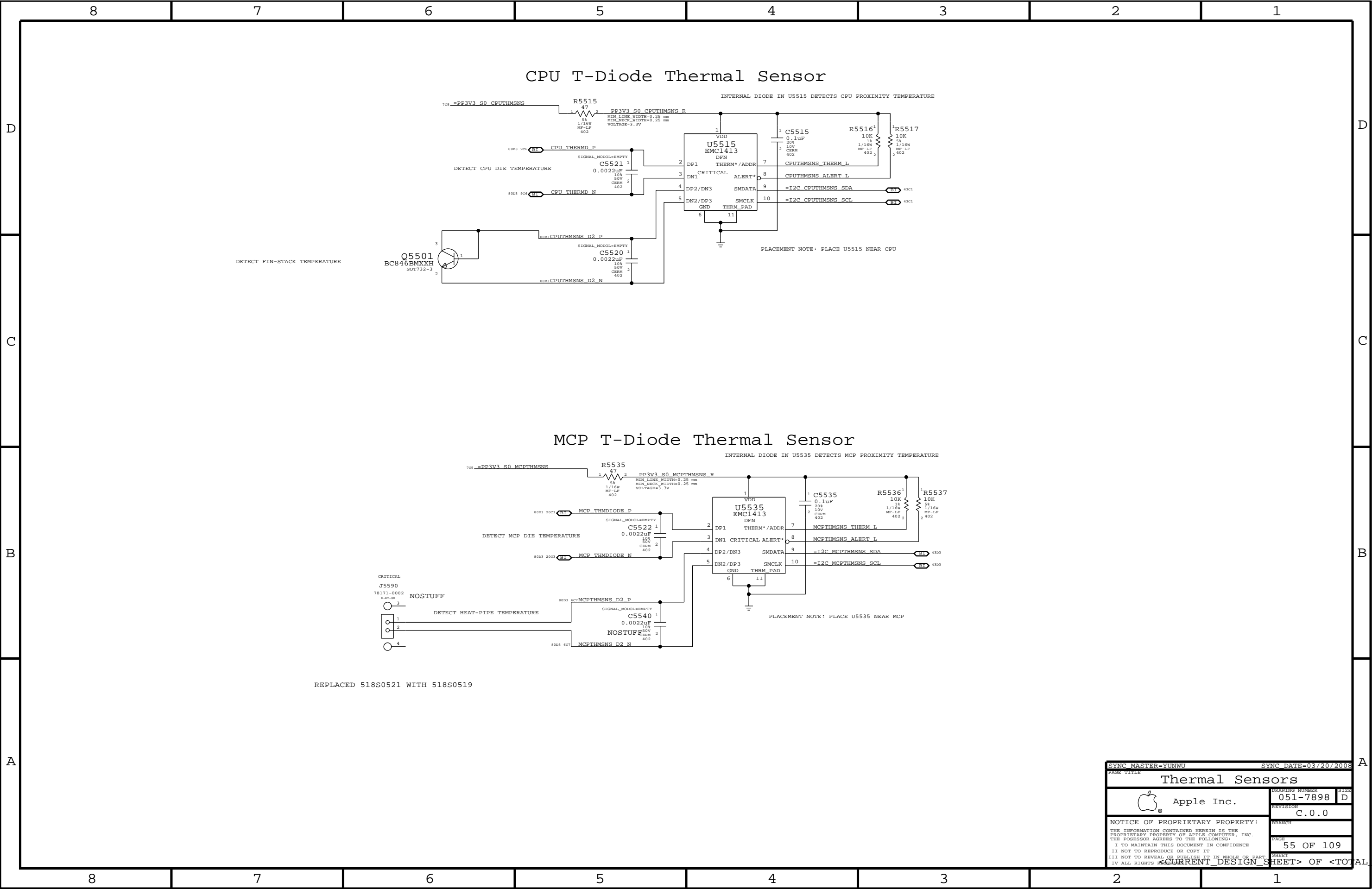
SYMC MASTER=CHANGZHANG		SYMC DATE=05/09/2008	
PAGE 11/18			
LPC+SPI Debug Connector			
 Apple Inc.	DRAWING NUMBER	SIZE	
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	REVISION		
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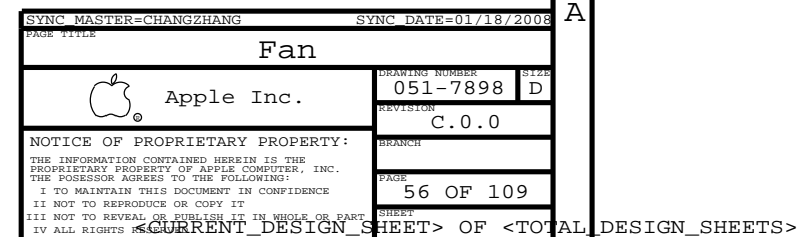


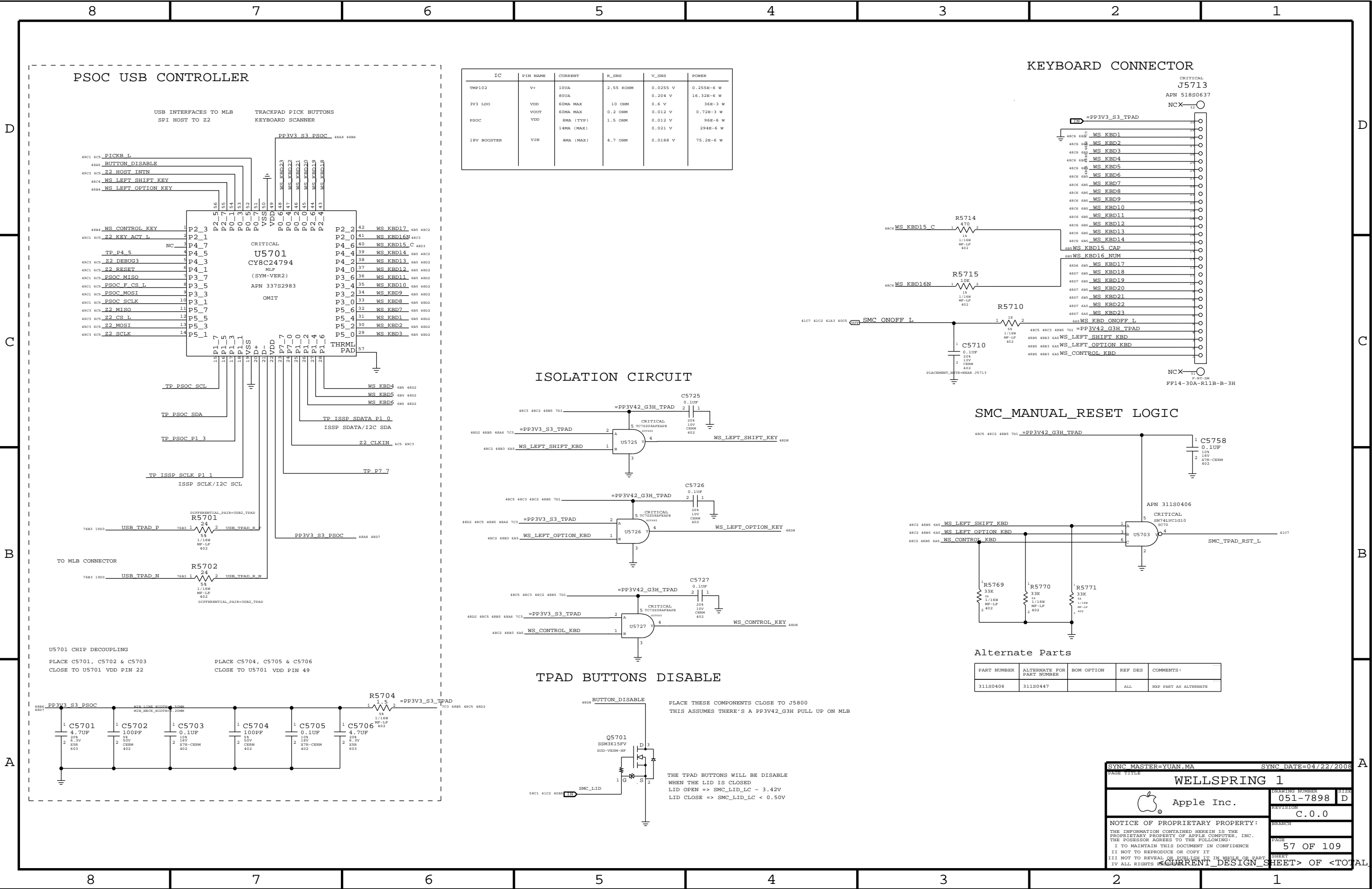


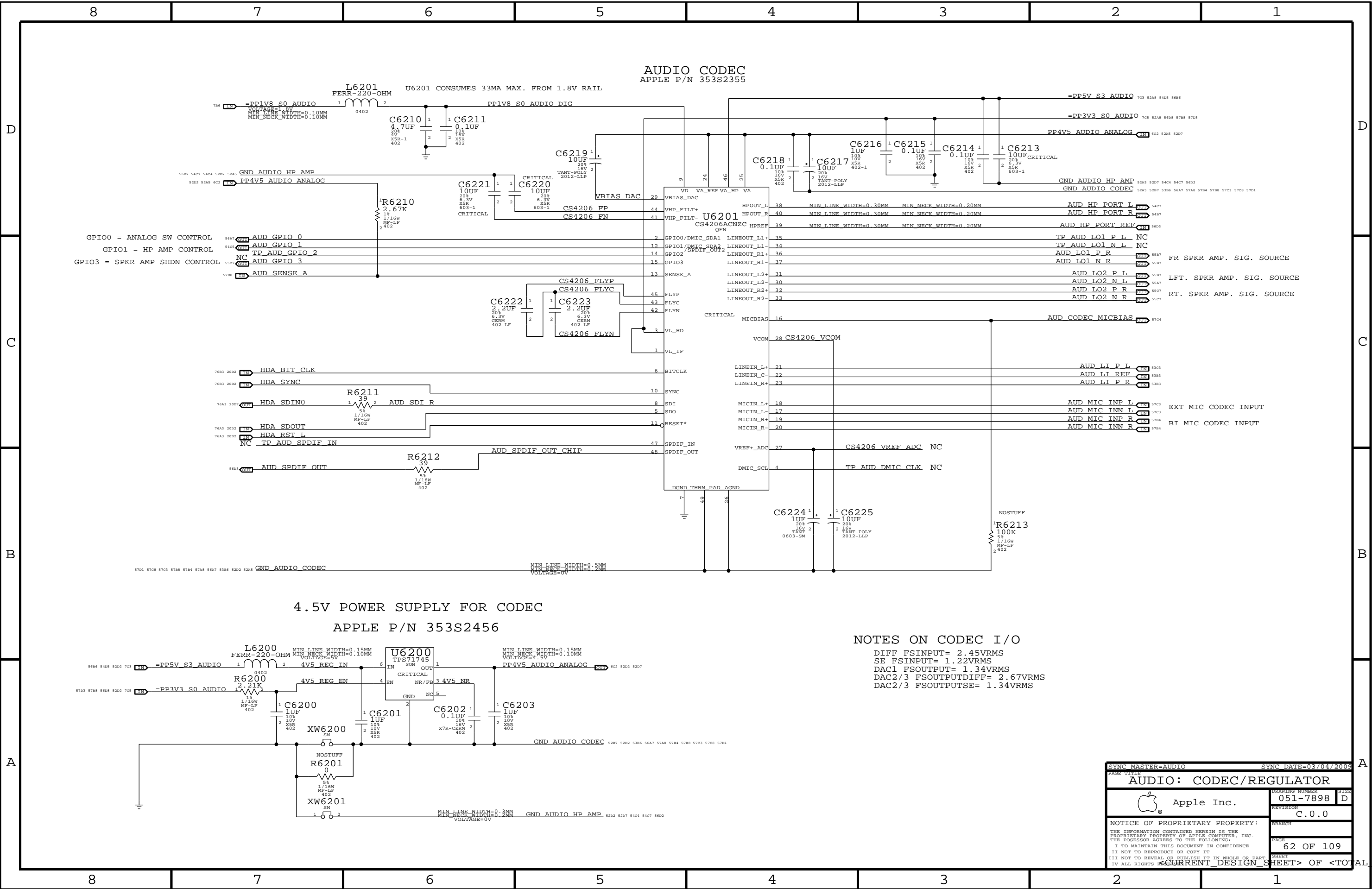
For engineering, stuff U5313 and unstuff R5330
For production, stuff R5330 and unstuff U5313

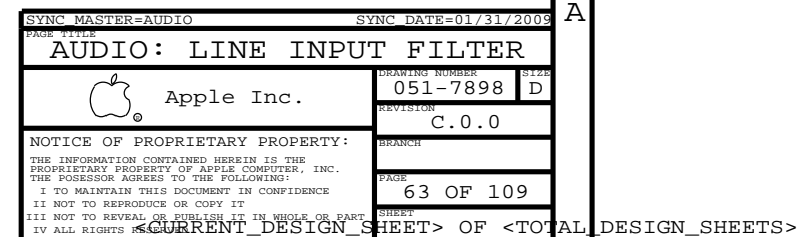
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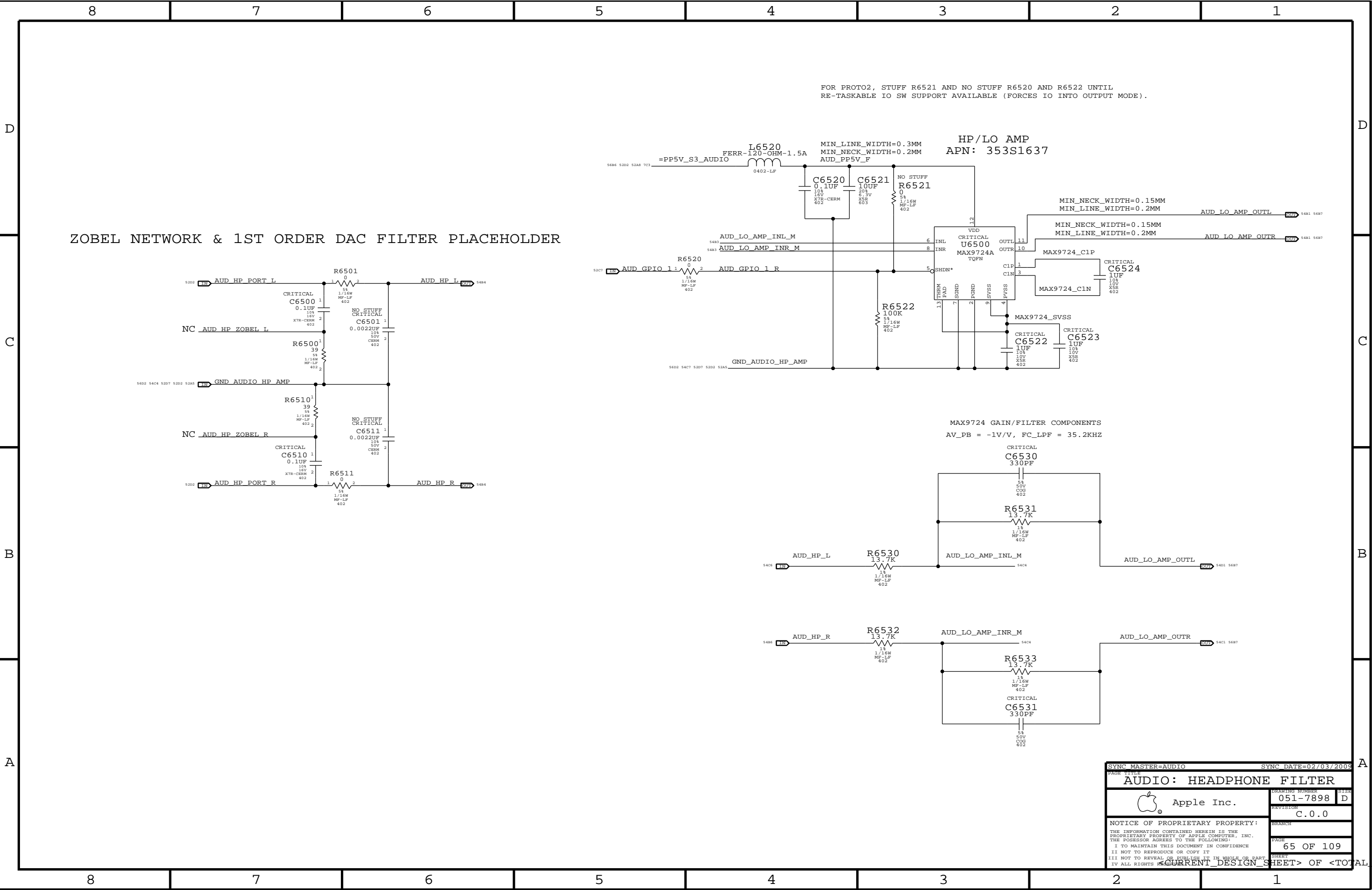






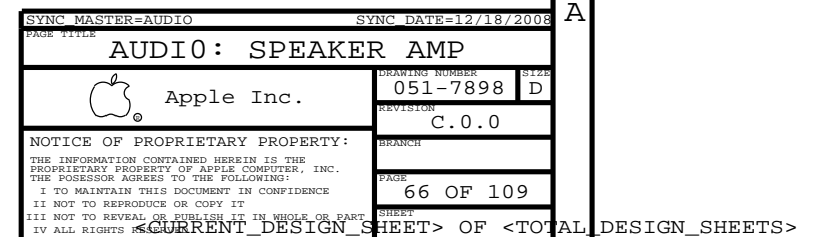


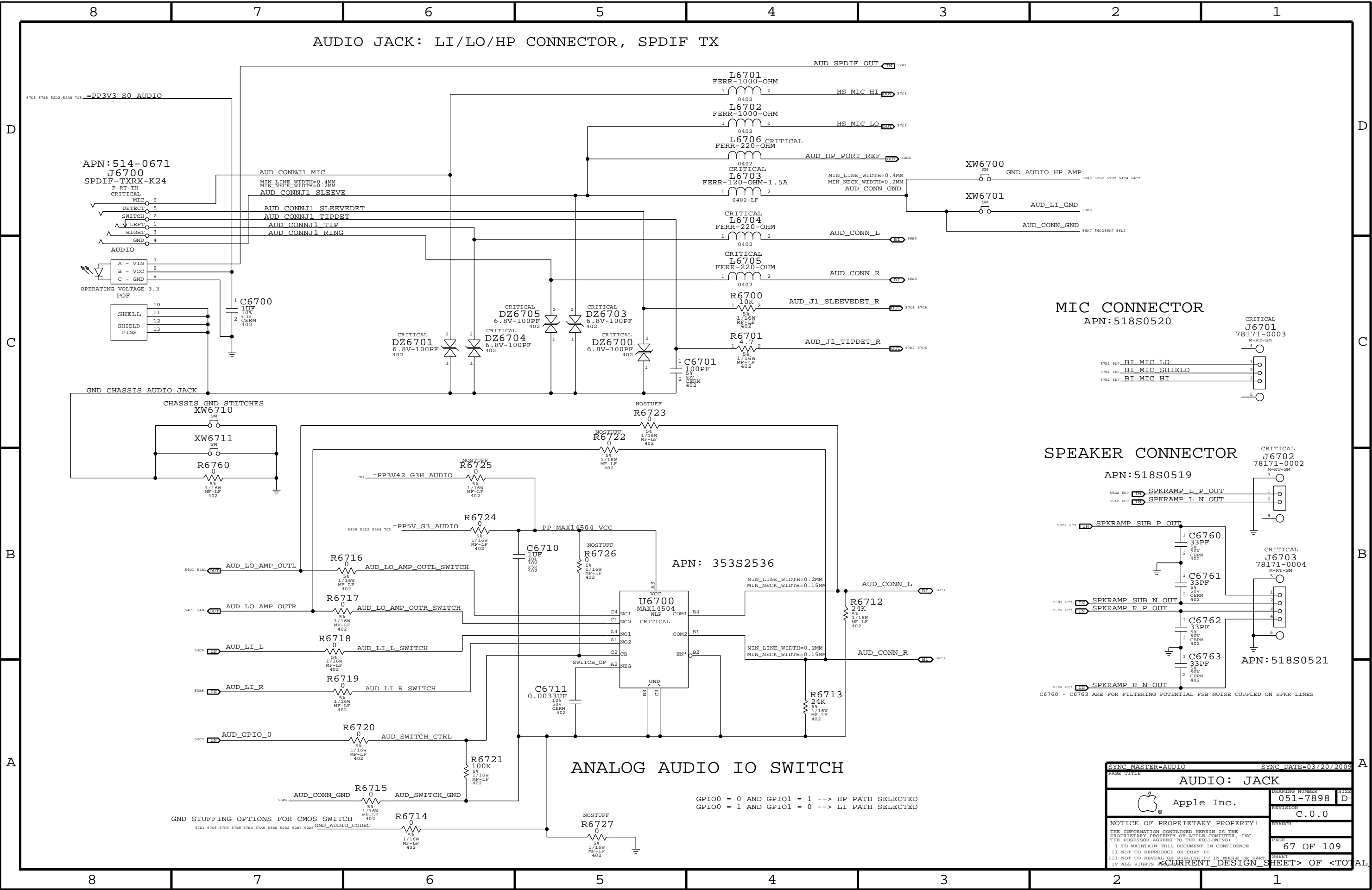





APN: 353S2524

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	6DB





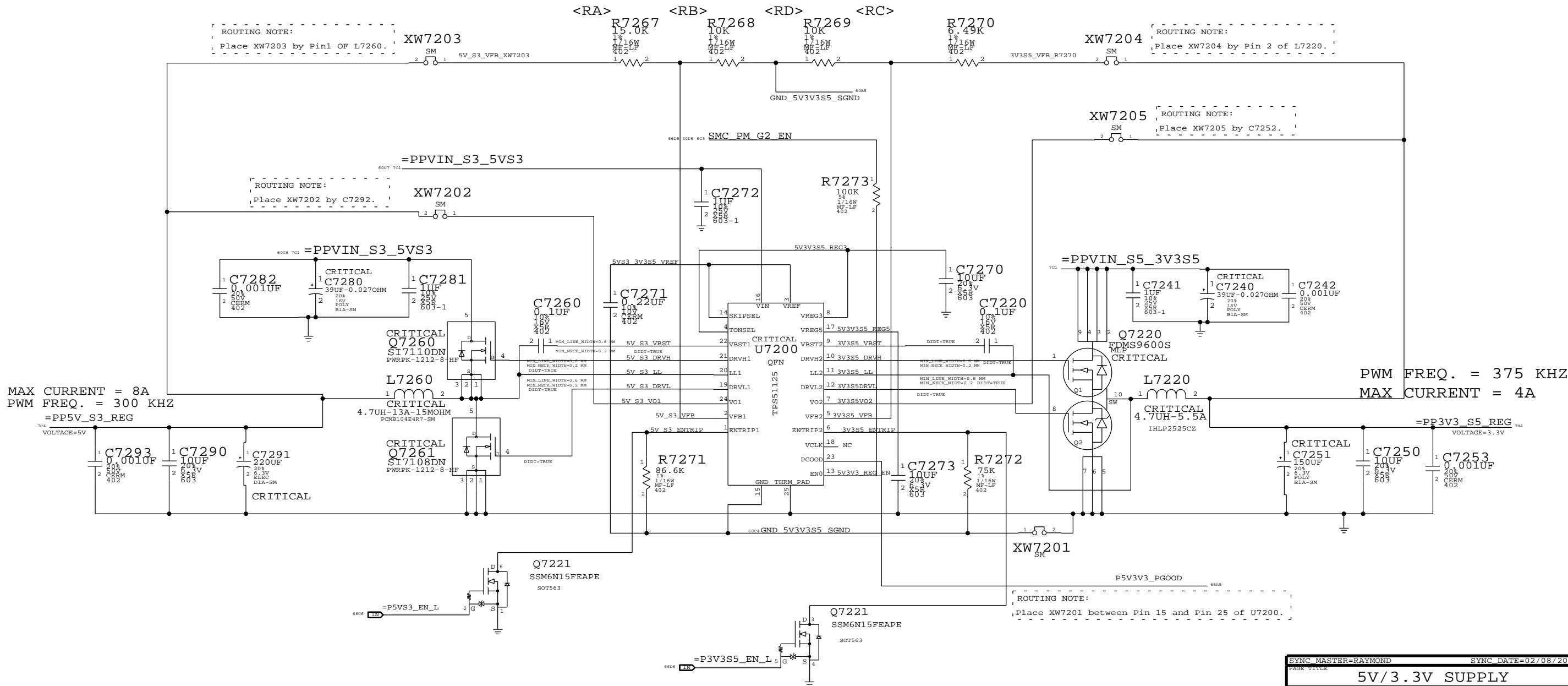
SYNC MASTER=AUDIO		SYNC DATE=03/20/2009	
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AUDIO: JACK			
	Apple Inc.		DRAWING NUMBER
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[illegible]

5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$



MAX CURRENT = 8A
PWM FREQ. = 300 KHZ
=PP5V_S3_REG

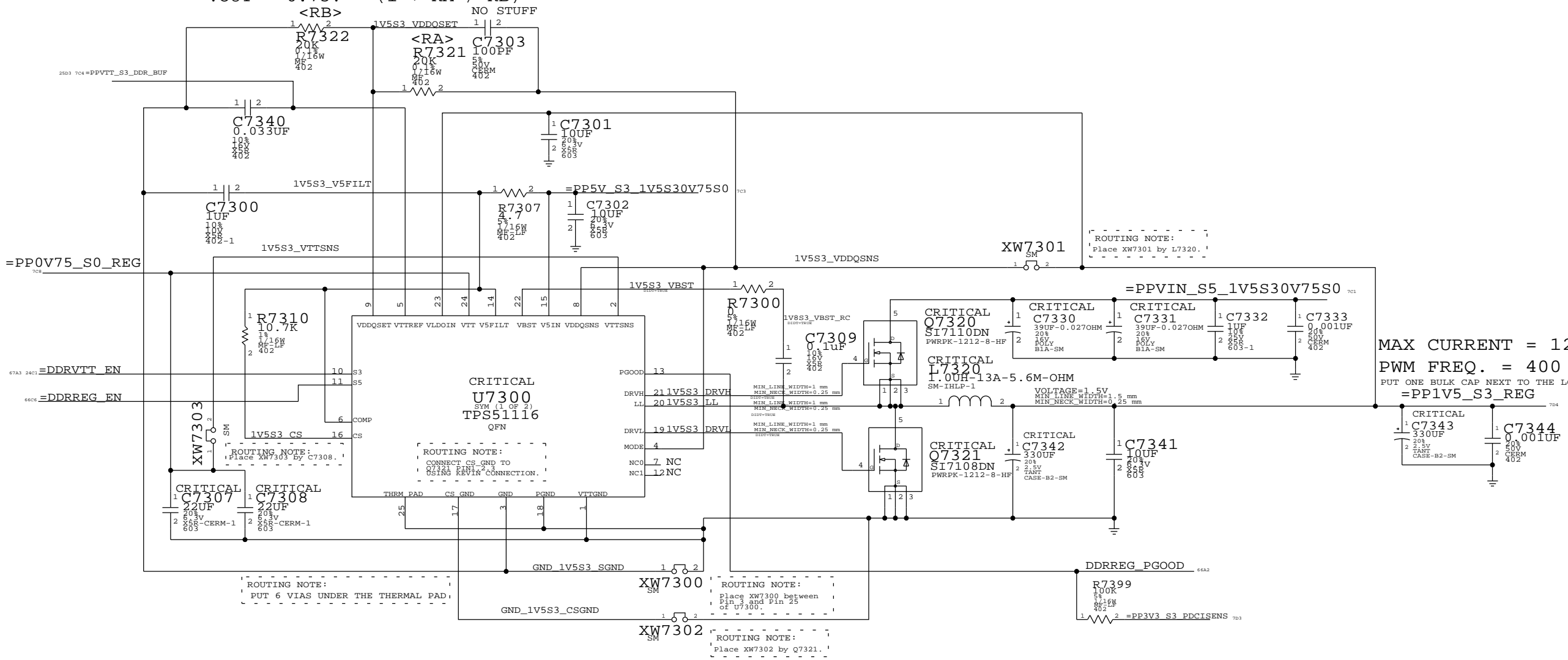
PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SEPERATED MASTER PG00D FOR BOTH 5V AND 3V3.

PAGE TITLE		PAGE NUMBER	
5V/3.3V SUPPLY		051-7898	
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1.5V/0.75V(DDR3) POWER SUPPLY

$$V_{OUT} = 0.75V * (1 + R_A / R_B)$$



MAX CURRENT = 12A
PWM FREQ. = 400 KHZ
PUT ONE BULK CAP NEXT TO THE LOAD
=PP1V5_S3_REG

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

SYNC MASTER=RAYMOND

SYNC DATE=01/31/2008

1.5V/0.75V DDR3 SUPPLY

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051-7898

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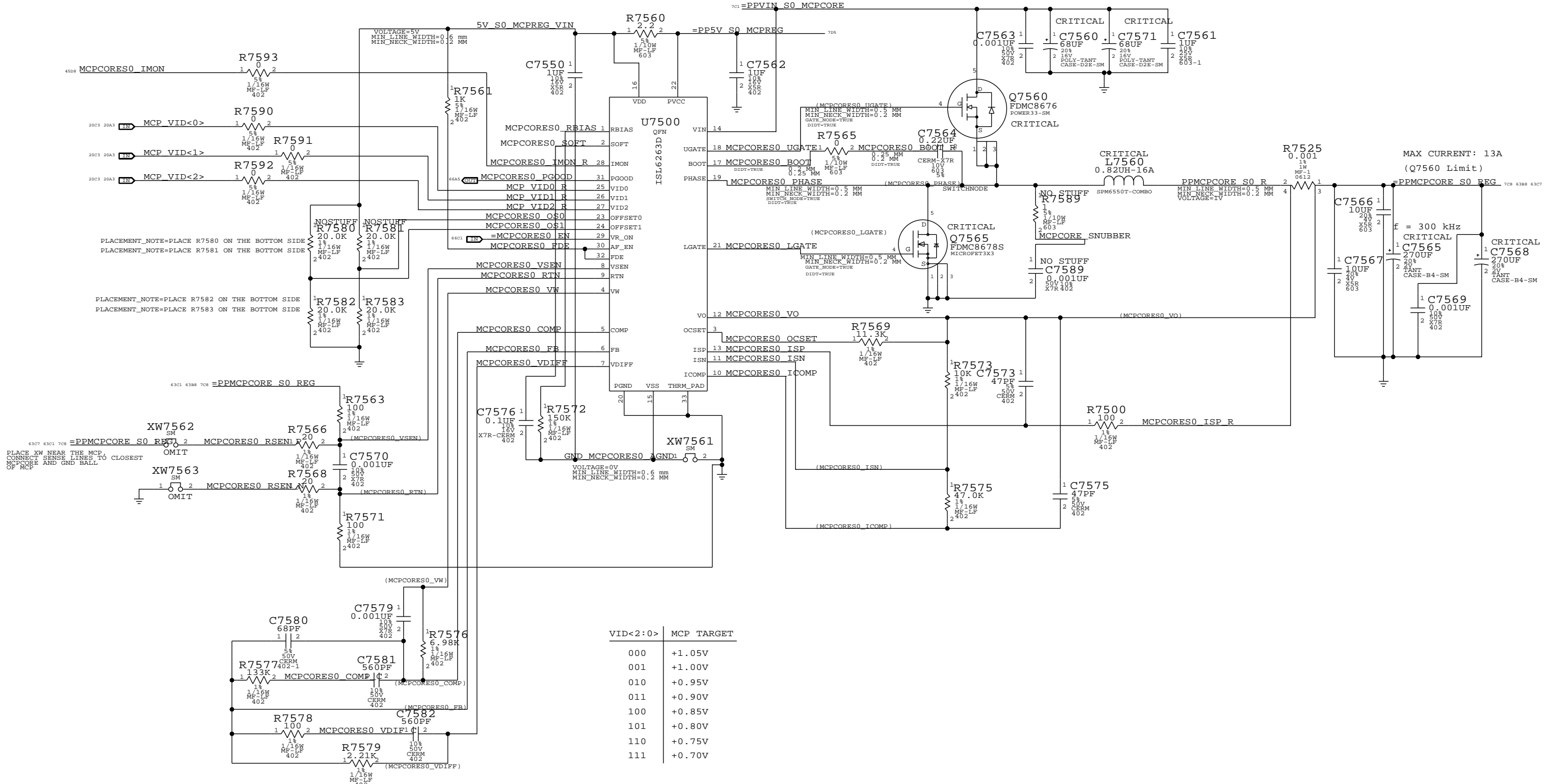
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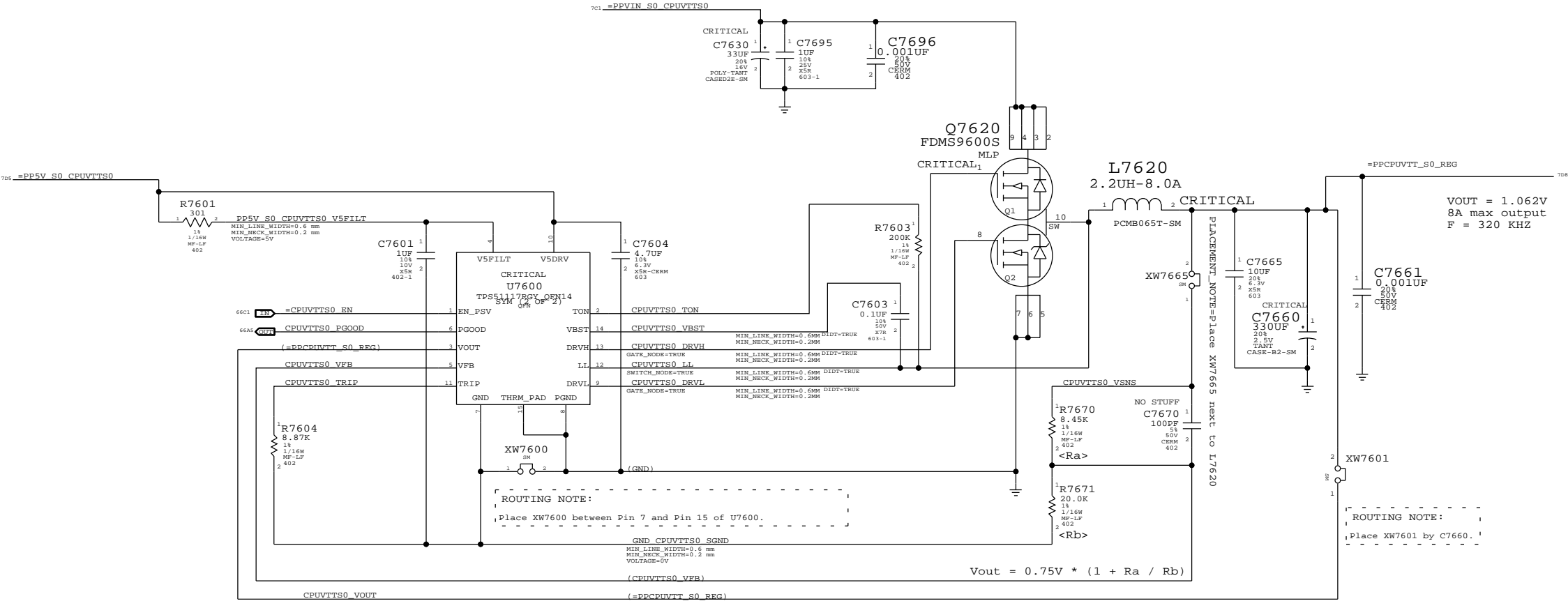
MCP VCORE POWER SUPPLY



VID<2:0>	MCP TARGET
000	+1.05V
001	+1.00V
010	+0.95V
011	+0.90V
100	+0.85V
101	+0.80V
110	+0.75V
111	+0.70V

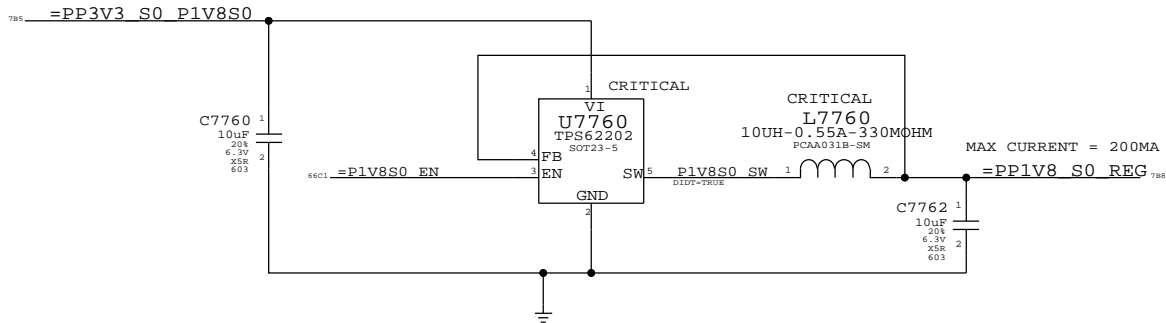
SYNC MASTER=K19 MLB		SYNC DATE=12/10/2008	
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MCP APPLE REGULATOR			
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CPUVTT POWER SUPPLY

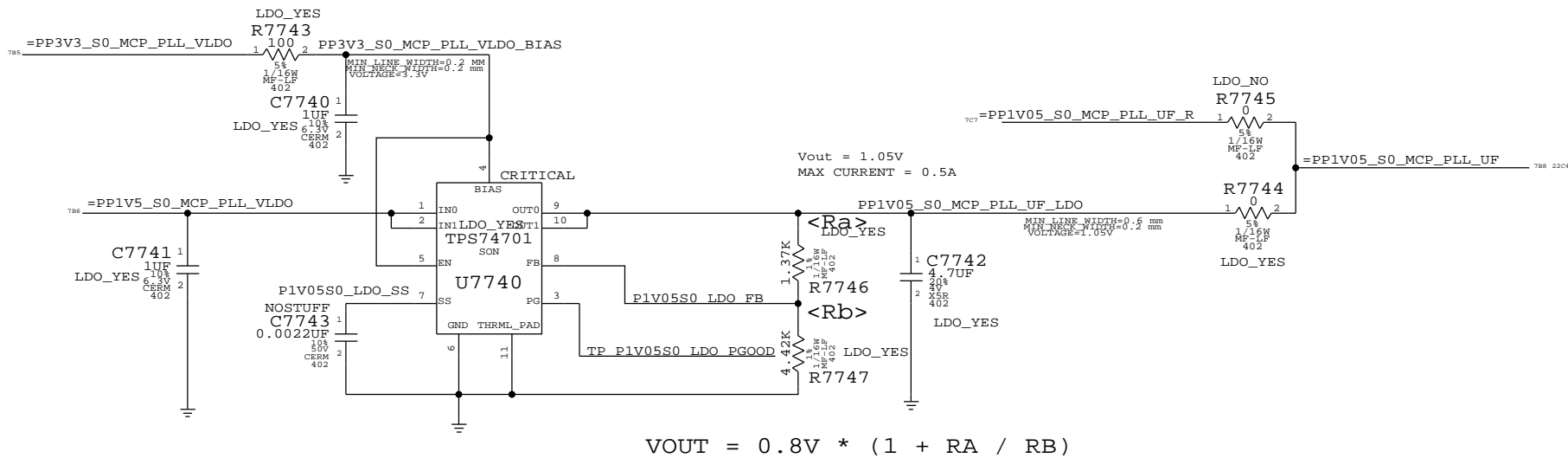


SYNC MASTER=RAYMOND		SYNC DATE=02/08/2008	
PAGE TITLE		CPU VTT(1.05V) SUPPLY	
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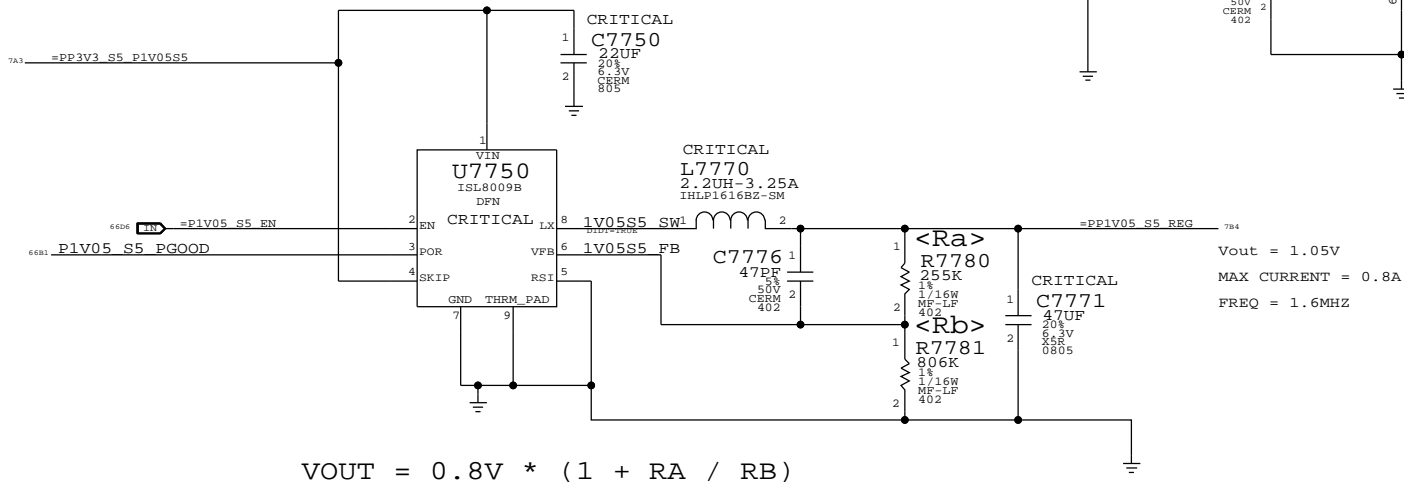
1.8V S0 SWITCHER



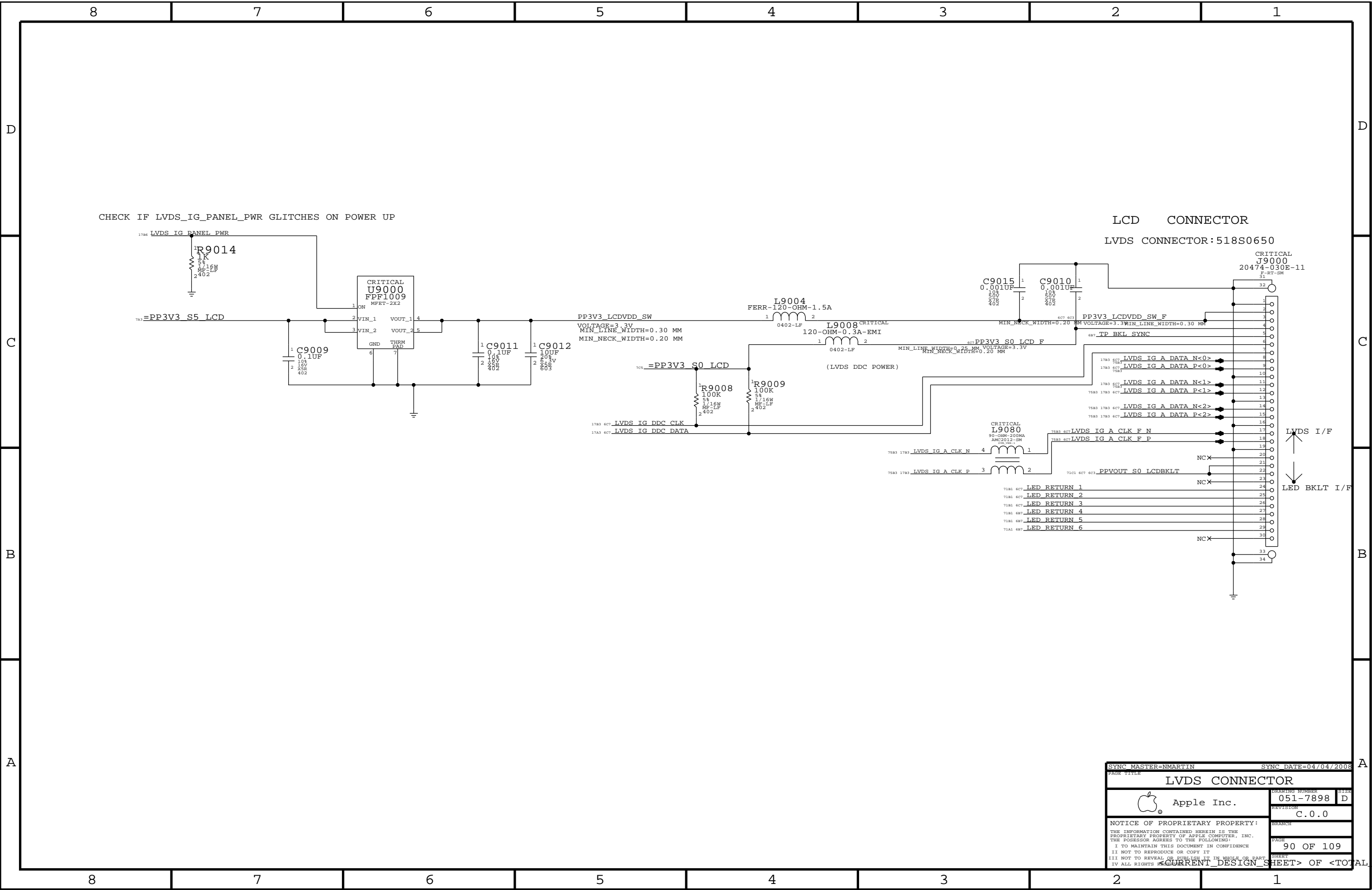
1.05V S0 PLL LDO




MCP 1.05V S5 (AUXC) SUPPLY

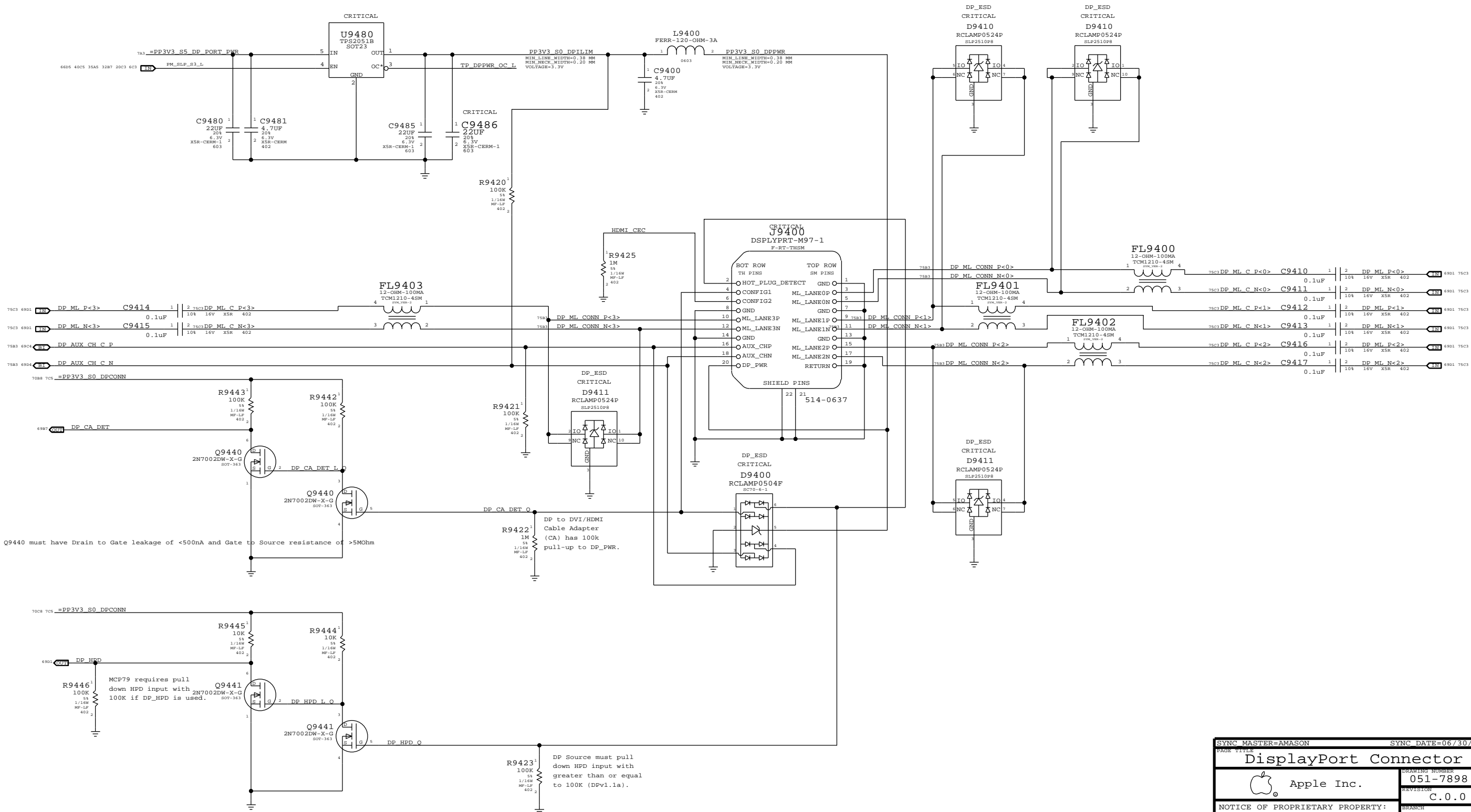



SYNC MASTER=RAYMOND		SYNC DATE=01/23/2008			
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MISC POWER SUPPLIES					
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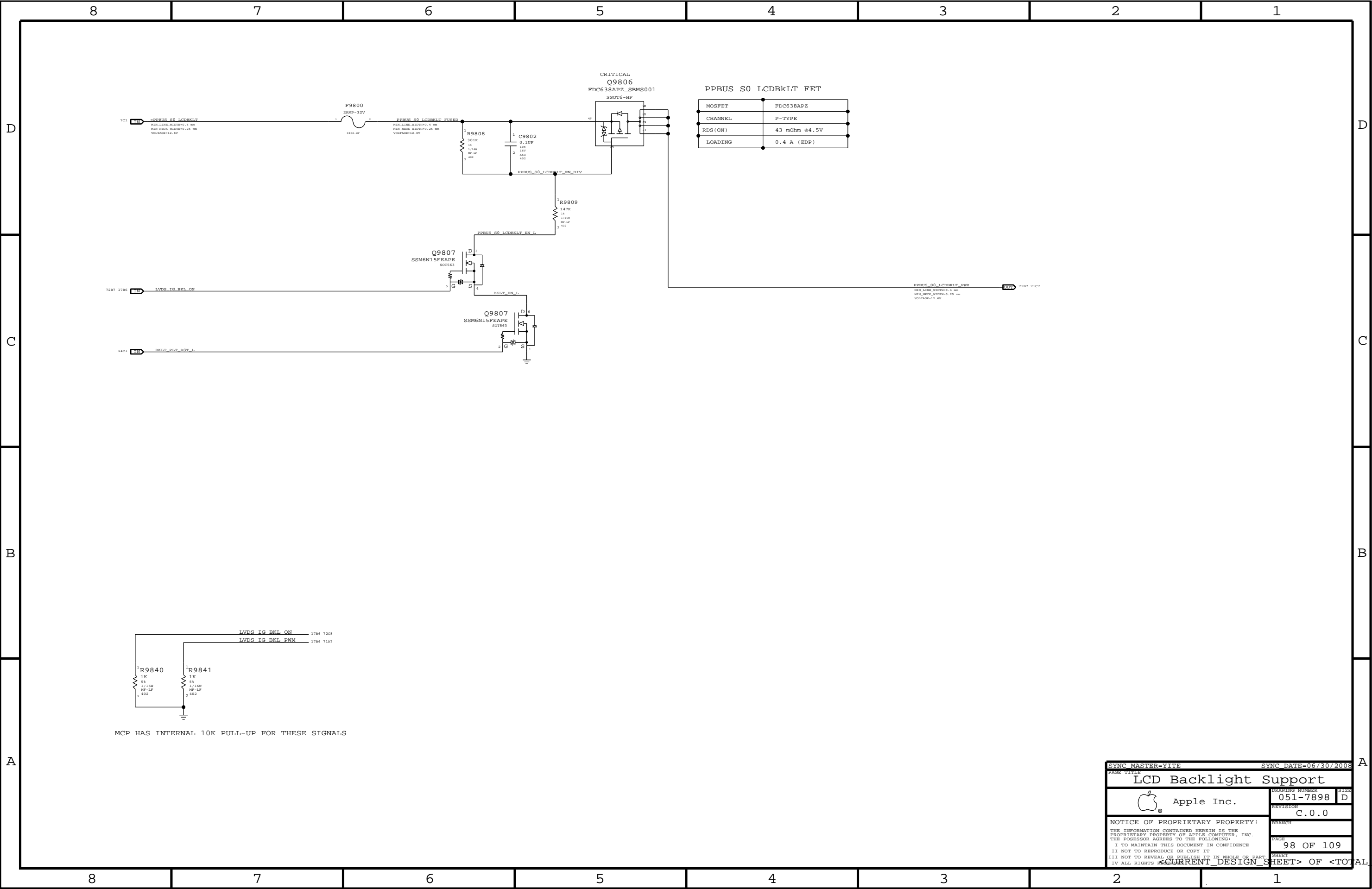


SYNC MASTER=NMARTIN		SYNC DATE=04/04/2008	
PAGE TITLE			
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Port Power Switch



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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFPAIR PRIMARY GAP	DIFFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFFPAIR	=1:1_DIFFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched to CPU clock, +/-1000 mils.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFPAIR PRIMARY GAP	DIFFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_SML	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFPAIR PRIMARY GAP	DIFFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFFPAIR PRIMARY GAP	DIFFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
		PHYSICAL	SPACING	
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0> 904 1303
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0> 904 1304
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0> 904 1304
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0> 904 1304
FSB 2X Signals	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16> 984 904 1303 1303
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1> 984 1304
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1> 984 1304
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1> 984 1304
FSB 1X Signals	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32> 902 1383 1303
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2> 902 1304
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2> 902 1304
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2> 902 1304
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48> 982 902 1383
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3> 982 1304
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3> 982 1304
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3> 982 1304
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3> 908 1304 1306
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REO L<4..0> 908 1386
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0> 908 1386
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17> 908 908 1306
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1> 908 1386
	FSB_1X	FSB_50S	FSB_1X	FSB ADS L 906 1386
	FSB_BREQ0 I	FSB_50S	FSB_1X	FSB BREQ0 L 906 1386
	FSB_BREQ1 I	FSB_50S	FSB_1X	FSB BREQ1 L 1386
	FSB_1X	FSB_50S	FSB_1X	FSB BNR L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB BPRI L 906 1383
	FSB_1X	FSB_50S	FSB_1X	FSB DBSY L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB DEFER L 906 1383
	FSB_1X	FSB_50S	FSB_1X	FSB DEDY L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB HIT L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB HITM L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB LOCK L 906 1386
	FSB_CPURST I	FSB_50S	FSB_1X	FSB CPURST L 906 1202 13A3
	FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0> 906 13A6
	FSB_1X	FSB_50S	FSB_1X	FSB TRDY L 906 1386
	FSB_1X	FSB_50S	FSB_1X	FSB TRDY L 906 1386
	CPU_ASYNC	CPU_50S	CPU_ASYNC	CPU A20M L 908 13A3
	CPU_BSEL	CPU_50S	CPU_ASYNC	CPU BSEL<2..0> 882 984
	CPU_FERR I	CPU_50S	CPU_SMTI	CPU FERR L 908 1387
	CPU_ASYNC	CPU_50S	CPU_ASYNC	CPU IGNEE L 908 13A3
	CPU_INIT I	CPU_50S	CPU_ASYNC	CPU INIT L 906 13A3
	CPU_ASYNC S	CPU_50S	CPU_ASYNC	CPU INTR 908 13A3
	CPU_ASYNC S	CPU_50S	CPU_ASYNC	CPU NMI 988 13A3
	CPU_PROCHOT I	CPU_50S	CPU_ASYNC	CPU PROCHOT L 905 1386 4104 6208
	CPU_PWRGD	CPU_50S	CPU_ASYNC	CPU PWRGD 982 1207 13A3
	CPU_ASYNC	CPU_50S	CPU_ASYNC	CPU SMI L 988 13A3
	CPU_ASYNC	CPU_50S	CPU_ASYNC	CPU STPCLK L 908 13A3
	PM_THERMTRIP I	CPU_50S	CPU_SMTI	PM THERMTRIP L 906 1387 4104
	FSB_CPUSLP I	CPU_50S	CPU_ASYNC	FSB CPUSLP L 982 13A3
	CPU_FERR SR	CPU_50S	CPU_ASYNC	CPU DPSLP L 982 13A3
	CPU_DPRSTP I	CPU_50S	CPU_ASYNC	CPU DPRSTP L 982 13A3 6207
	CPU_ASYNC	CPU_50S	CPU_ASYNC	FSB DPWR L 982 13A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD 13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND 13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC 13A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND 13A6
	FSB_CLK_CPU0	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P 986 1383
	FSB_CLK_CPU1	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N 986 1383
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P 1203 1383
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N 1203 1383
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P 13A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N 13A4
	CPU_IERR I	CPU_50S		CPU IERR L 906
	PM DPRSLPVR	CPU_50S	CPU_ASYNC	PM DPRSLPVR 2007 6208
	(See above)	CPU_50S	CPU_ASYNC	IMVP DPRSLPVR 6207
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF 984 2581
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3> 983
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2> 983
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1> 983
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0> 983
	XDP_TDI	CPU_50S	CPU_ITP	XDP TDI 986 906 1283
	XDP_TDO	CPU_50S	CPU_ITP	XDP TDO 986 906 1283
	XDP_TMS	CPU_50S	CPU_ITP	XDP TMS 986 906 1283
	XDP_TCK	CPU_50S	CPU_ITP	XDP TCK 9A6 906 1286
	XDP_TRST I	CPU_50S	CPU_ITP	XDP TRST L 9A6 906 1283
	XDP_BM I	CPU_50S	CPU_ITP	XDP BM L<4..0> 906 1206
	XDP_BM I<5	CPU_50S	CPU_ITP	XDP BM L<5> 905 1206
	(FSB_CPURST I)	CPU_50S	CPU_ITP	XDP CPURST L 1204
		CPU_50S	CPU_SMTI	CPU VID<6..0> 1086 6207
		CPU_50S	CPU_SMTI	IMVP6 VID<6..0> 1086 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P 10A5 62A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N 10A5 62A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N

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CPU/FSB Constraints

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	8	7	6	5	4	3	2	1							
D	PCI Bus Constraints								D						
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
	PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
	CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD							
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT											
	PCI	*	=STANDARD	?											
	CLK_PCI	*	8 MIL	?											
	SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.														
	LPC Bus Constraints														
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT												
LPC	*	6 MIL	?												
CLK_LPC	*	8 MIL	?												
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.															
USB 2.0 Interface Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD								
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.															
SMBus Interface Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT												
SMB	*	=2x_DIELECTRIC	?												
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.															
HD Audio Interface Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT												
HDA	*	=2x_DIELECTRIC	?												
MCP_HDA_COMP	*	8 MIL	?												
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.															
SIO Signal Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT												
CLK_SLOW	*	8 MIL	?												
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.															
SPI Interface Constraints															
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP								
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD								
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT												
SPI	*	8 MIL	?												
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.															

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUFO_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4


88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
0000	MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	1706
0000	MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	1706
0000	MCP_CLK25M_BUFD	ENET_MII_55G	MCP_BUFD_CLK	MCP_CLK25M_BUFD_R	1703 3245
0000		ENET_MII_55G	MCP_BUFD_CLK	RTL8211_CLK25M_CKXTAL1	3186 3243
0000	ENET_INTR_L	ENET_MII_55G	ENET_MII	ENET_INTR_L	
0000	ENET_MDIO	ENET_MII_55G	ENET_MII	ENET_MDIO	1703 3186
0000	ENET_MDC	ENET_MII_55G	ENET_MII	ENET_MDC	1703 3186
0000	ENET_PWDOWN_L	ENET_MII_55G	ENET_MII	ENET_PWRDWN_L	
0000		ENET_MII_55G	ENET_MII	ENET_CLK125M_EXCLK_R	3104
0000	ENET_RXCLK	ENET_MII_55G	ENET_MII	ENET_CLK125M_EXCLK	1706 3101
0000		ENET_MII_55G	ENET_MII	ENET_RXD_R<3..0>	3104
0000	ENET_RXD	ENET_MII_55G	ENET_MII	ENET_RXD<0>	1706 3101
0000	ENET_RXD_STRAP	ENET_MII_55G	ENET_MII	ENET_RXD<3..1>	1706 3101
0000	ENET_RXD	ENET_MII_55G	ENET_MII	ENET_RX_CTRL	1706 3181
0000		ENET_MII_55G	ENET_MII	ENET_RXCTL_R	3184
0000		ENET_MII_55G	ENET_MII	ENET_CLK125M_TXCLK_R	3106
0000	ENET_TXCLK	ENET_MII_55G	ENET_MII	ENET_CLK125M_TXCLK	1703 3108
0000	ENET_TXD0	ENET_MII_55G	ENET_MII	ENET_TXD<0>	1703 3106
0000	ENET_TXD	ENET_MII_55G	ENET_MII	ENET_TXD<3..1>	1703 3106
0000	ENET_TXD	ENET_MII_55G	ENET_MII	ENET_TX_CTRL	1703 3186
0000		ENET_MII_55G	ENET_MII	ENET_RESET_L	1703 3187
0000	ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	3183 3388 3308
0000		ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	3183 3388 3308
0000		ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0>	3184 3304 3305
0000		ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0>	3184 3304 3305

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Ethernet Constraints									
 Apple Inc.	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">DRAWING NUMBER</td> <td style="width: 40%;">SIZE</td> </tr> <tr> <td style="text-align: center;">051-7898</td> <td style="text-align: center;">D</td> </tr> <tr> <td colspan="2">REVISION</td> </tr> <tr> <td colspan="2" style="text-align: center;">C.0.0</td> </tr> </table>	DRAWING NUMBER	SIZE	051-7898	D	REVISION		C.0.0	
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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110	*	<=10_00MLDIFF	<=10_00MLDIFF	<=10_00MLDIFF	<=10_00MLDIFF	<=10_00MLDIFF	<=10_00MLDIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_10	*	<=312_SPACING	5

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55	*	<=55_00MLSE	<=55_00MLSE	<=55_00MLSE	<=55_00MLSE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	<=38_01ELECTRIC	7

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE				
		PHYSICAL	SPACING			
	FW_P0_TPA_P	FW_1100	FW_TE	FW_P0_TPA_P	3486	3404
	FW_P0_TPA_N	FW_1100	FW_TE	FW_P0_TPA_N	3406	3404
	FW_P0_TPB_P	FW_1100	FW_TE	FW_P0_TPB_P	3486	3404
	FW_P0_TPB_N	FW_1100	FW_TE	FW_P0_TPB_N	3486	3404
	FW_P1_TPA_P	FW_1100	FW_TE	FW_P1_TPA_P	3486	3488
	FW_P1_TPA_N	FW_1100	FW_TE	FW_P1_TPA_N	3486	3488
	FW_P1_TPB_P	FW_1100	FW_TE	FW_P1_TPB_P	3486	3488
	FW_P1_TPB_N	FW_1100	FW_TE	FW_P1_TPB_N	3486	3488
Port 2 Not Used						

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	SD_D<0>	SD_55S	SD_INTERFACE	SD_D<0>	3002
	SD_D<1>	SD_55S	SD_INTERFACE	SD_D<1>	3002
	SD_D<2>	SD_55S	SD_INTERFACE	SD_D<2>	3002
	SD_D<3>	SD_55S	SD_INTERFACE	SD_D<3>	3002
	SD_D<4>	SD_55S	SD_INTERFACE	SD_D<4>	3002
	SD_D<5>	SD_55S	SD_INTERFACE	SD_D<5>	3002
	SD_D<6>	SD_55S	SD_INTERFACE	SD_D<6>	3002
	SD_D<7>	SD_55S	SD_INTERFACE	SD_D<7>	3002
	SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	3002
	SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	3002

FireWire Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SMBUS SMC A S3 SCL	SMB_55G	SMB	SMBUS SMC A S3 SCL	605 605 4302
SMBUS SMC A S3 SDA	SMB_55G	SMB	SMBUS SMC A S3 SDA	605 605 4302
SMBUS SMC B S0 SCL	SMB_55G	SMB	SMBUS SMC B S0 SCL	4302
SMBUS SMC B S0 SDA	SMB_55G	SMB	SMBUS SMC B S0 SDA	4302
SMBUS SMC 0 S0 SCL	SMB_55G	SMB	SMBUS SMC 0 S0 SCL	4305
SMBUS SMC 0 S0 SDA	SMB_55G	SMB	SMBUS SMC 0 S0 SDA	4305
SMBUS SMC BSA SCL	SMB_55G	SMB	SMBUS SMC BSA SCL	6A7 4305
SMBUS SMC BSA SDA	SMB_55G	SMB	SMBUS SMC BSA SDA	6A7 4305
SMBUS SMC MGMT SCL	SMB_55G	SMB	SMBUS SMC MGMT SCL	4385
SMBUS SMC MGMT SDA	SMB_55G	SMB	SMBUS SMC MGMT SDA	4385

SMBus Charger Net Properties

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CHGR CSI+	1TO1_DIFFPAIR		CHGR CSI P	
CHGR CSI-	1TO1_DIFFPAIR		CHGR CSI N	
CHGR CSO	1TO1_DIFFPAIR		CHGR CSO P	
CHGR CSO	1TO1_DIFFPAIR		CHGR CSO N	

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SMC Constraints

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